SCHEME & SYLLABUS OF M.TECH ECE EFFECTIVE FROM 2012-13
<table>
<thead>
<tr>
<th>Sr.No</th>
<th>Course No.</th>
<th>Course Title</th>
<th>Teaching Schedule</th>
<th>Marks of Class Work</th>
<th>Exam. Marks</th>
<th>Total Marks</th>
<th>Credit</th>
<th>Duration of Exam.</th>
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<tbody>
<tr>
<td>1</td>
<td>MTEC-501-B</td>
<td>Advanced Digital Signal Processing</td>
<td>4 L - 0 P</td>
<td>25 Theory</td>
<td>75 Practical</td>
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<td>2</td>
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<td>Information &amp; Communication Theory</td>
<td>4 L - 0 P</td>
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<td>4 L - 0 P</td>
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<tr>
<td>4</td>
<td>MTEC-507-B</td>
<td>Advance Microprocessor &amp; Application</td>
<td>4 L - 0 P</td>
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<td>5</td>
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<td>Optimization Techniques</td>
<td>4 L - 0 P</td>
<td>25 Theory</td>
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<td>6</td>
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<td>Digital VLSI Design Lab</td>
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<td>7</td>
<td>MTEC-537-B</td>
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</table>

Note:

1. The students will be allowed to use non-Programmable Scientific Calculator. However, sharing/exchange of calculator are prohibited in the examination.
2. Electronics Gadgets including Cellular Phones are not allowed in the examination.
### SEMESTER II

<table>
<thead>
<tr>
<th>Sr.No</th>
<th>Course No.</th>
<th>Course Title</th>
<th>Teaching Schedule</th>
<th>Marks of Class Work</th>
<th>Exam. Marks</th>
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<td></td>
<td>MTEC-502-B</td>
<td>Advanced Electronics Instrumentation</td>
<td>4 - 25</td>
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**Total**

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**ELECTIVE – I**

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<tr>
<th>MTEC-508-B</th>
<th>Analog VLSI Design</th>
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<tr>
<td>MTEC-510-B</td>
<td>Multimedia Communication</td>
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<tr>
<td>MTEC-512-B</td>
<td>Statistical Signal Processing</td>
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<tr>
<td>MTEC-514-B</td>
<td>Design of Embedded system</td>
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<td>MTEC-516-B</td>
<td>Embedded Networking</td>
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**ELECTIVE – II**

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<thead>
<tr>
<th>MTEC-518-B</th>
<th>Semiconductor Device Modeling</th>
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<tr>
<td>MTEC-520-B</td>
<td>Advanced Satellite Communication</td>
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<tr>
<td>MTEC-522-B</td>
<td>Multirate and Wavelet signal Processing</td>
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<td>MTEC-524-B</td>
<td>DSP Processor</td>
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<td>MTEC-526-B</td>
<td>Communication Network</td>
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1. The students will be allowed to use non-Programmable Scientific Calculator. However, sharing/exchange of calculator are prohibited in the examination.
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## SEMESTER III

<table>
<thead>
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<th>Sr.No</th>
<th>Course No.</th>
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<th>Exam. Marks</th>
<th>Total Marks</th>
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<td>Advanced Wireless Communication System</td>
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<td>Reliability Engineering</td>
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### ELECTIVE 3

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<tr>
<td>MTEC-605-B</td>
<td>CMOS Mixed signal circuit design</td>
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<tr>
<td>MTEC-607-B</td>
<td>MEMS and IC Integration</td>
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<tr>
<td>MTEC-609-B</td>
<td>Algorithm for VLSI Design</td>
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<tr>
<td>MTEC-611-B</td>
<td>Software for Embedded System</td>
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<tr>
<td>MTEC-613-B</td>
<td>Embedded Application Based on Advance Microcontroller</td>
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</tbody>
</table>

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DEENBANDHU CHHOTU RAM UNIVERSITY OF SCIENCE & TECHNOLOGY, MURTHAL (SONEPAT)
### SEMESTER IV

<table>
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</table>

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UNIT I

Sampling and Multi rate Digital Signal Processing:
Sampling: Review of Basic Sampling theorem, Sampling for Band limited Signals with sampling rate less than twice of maximum frequency, Integer band positioning, Arbitrary band positioning, Reconstruction, sampling rate conversion.
Multi rate Signal Processing (MSP): Need for MSP, Increasing & Decreasing sampling rate by integer factor (Interpolation & Decimation), Changing the sampling rate by rational factor, Structures for sampling rate conversion: Polyphase Filter implementation, cascaded integrator comb Filters; Multistage Structures, Applications of MSP.

UNIT II

Linear Prediction & Optimum Linear Filters:
Stationary Random Process Representation: AR, MA & ARMA Processes, autocorrelation sequence and filter coefficients association; Linear Prediction: Backward & Forward; Optimum Reflection coefficients for lattice backward & forward predictors, AR process and linear prediction Relationship.

UNIT III

Power Spectrum Estimation:

UNIT IV

Finite word length effects and DSP applications:
Finite word length effects in Digital Filters: Number Representation Systems: Binary, Fixed Point Arithmetic, Floating Point Arithmetic, Number Quantization, Error due to coefficient quantization, Low Sensitive Realizations, Quantization of product, Signal Scaling, Output Round off Noise Minimization, Limit Cycle Oscillations.

Text Books:

Reference Books:

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I

Field Algebra: Introduction, Binary operations, Groups, Characteristics of the field, Binary field arithmetic, Galois field, vector spaces, matrices.

Block Codes: Linear block codes, The Generator & parity check matrices, Syndrome decoding, Hamming codes, BCH codes, Reed Solomon codes, Justeen codes, MDS code, Reed Muller Code.

UNIT II

Channel Coding: Waveform Coding, types of error control, structured sequences, error detecting and correcting capability, usefulness of standard array, cyclic codes, interleaving and concatenated codes, coding and interleaving applied to the compact disc, turbo codes.

Source Coding: Sources, amplitude quantizing, adaptive prediction, transform coding, source coding for digital data, examples of source coding.

UNIT III

Modulation and coding tradeoffs: Goals of communication system designer, error probability plane, Nyquist minimum bandwidth, Shannon Hartley capacity theorem, bandwidth efficiency plane, modulation and coding tradeoffs, designing and evaluating digital communication systems, bandwidth efficient modulation, modulation and coding for band limited channels, trellis coded modulation.


UNIT IV

Estimation and Hypothesis Testing: Time and Ensemble Averages, Covariance and Correction Functions. Simple binary hypothesis tests, Decision Criteria, Neyman Pearson tests, Bayes Criteria, Multiple Hypothesis testing, Composite hypothesis testing, Asymptotic Error rate of LRT for simple hypothesis testing.


Text Books:
4. Taub Schilling, Principles of Communication Systems
5. Harry L Vantrees, Detection , Estimation and modulation Theory A Willey Interscience Publication

Reference Books:

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I
Introduction: VLSI Design flow, Design hierarchy, VLSI design style, computer - Aided Design Technology, Basic principle of MOS transistor, Introduction to large signal MOS models for digital design, geometric scaling theory, small device models and effects. 
The MOS Inverter: Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Latch-up, Propagation Delay and Power Consumption.

UNIT II

UNIT III
Combinational Logic Structures: CMOS Logic Families - static, dynamic and differential logic families, CMOS Complimentary logic, Pseudo NMOS logic, Dynamic CMOS logic, CMOS Domino logic, Clocked CMOS logic, pass Transistor logic, transmission gates logic circuits, complimentary switch logic. 

UNIT IV
Subsystem Design: Design of an ALU Subsystem: design 4-bit simple and carry look ahead adder, multiplier design: serial-parallel multiplier, Braun Array, Wallace tree Multiplier, Design of 4-bit Shifter.
Low Power CMOS Logic: overview of power consumption, Low power design: Voltage Scaling, optimization of switching activity.

Text Books:

Reference Books:
3. John P.Uyemura, CMOS Logic Circuit Design

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I

DESIGN OF MICROPROCESSOR: Design of basic microprocessor architectural Concepts: Microprocessor architecture, word Lengths, addressable memory, and Microprocessor's speed architectural characteristics, registers, instruction, memory addressing architecture, ALU, GPR's Control logic & internal data bus.

MICROPROCESSOR INSTRUCTIONS & COMMUNICATION: Instruction Set, Mnemonics, Basic Instruction Types, Addressing modes, Microprocessor I/O connecting I/O put to Microprocessor, Polling and Interrupts, Interrupt and DM. Controllers.

UNIT II

ADVANCED MICROPROCESSOR: Advanced microprocessors: Intel X86 family of advanced Microprocessor, programming model of 86 families, X86 addressing modes, instruction set, hardware.

HIGH PERFORMANCE CISC ARCHITECTURE (PENTIUM): The software model, functional description, CPU pin descriptions, RISC concepts, bus operations, super scalar architecture, pipe-lining, Branch prediction.

UNIT III

PENTIUM PROCESSOR: The instruction and caches, Floating point unit, protected mode operation, Segmentation, paging, multitasking, Exception and interrupts, Input / Output, Virtual 8086 model, Interrupt processing.

INSTRUCTIONS & PROGRAMMING WITH PENTIUM PROCESSOR: Instruction types, Addressing modes, Processor flags, Instruction set, Basic programming the Pentium Processor.

UNIT IV

PENTIUM PROCESSOR I/O: Data Communication, parallel I/O serial communication, Serial interface and UART modem, I/O devices, D/A, A/D interface, special I/O devices.

DEVELOPING PENTIUM PROCESSOR BASED APPLICATIONS: Introduction to the Design Process, Preparing the specifications, Developing a design, Implementing and Testing and design, Regulatory Compliance Testing, design tool for Development.

Text and Reference Books:

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I

Introduction: Operation Research Models, OR Model, Queuing & Simulation Models, Two Variable LP Model, Graphical LP solution, Computer Solution with solver & AMPL, Linear Programming Applications.


UNIT II


UNIT III


Queuing Models: Elements of Queuing Model, Role of Exponential Distribution, Pure Birth & Death Model, Specialized Poisson Queues, P-K Formula, Queuing Decision Models.

UNIT IV

Simulation Modeling: Monte Carlo Simulation, Type of Simulations, Unconstrained Problems, Constrained Problems, Direct Search Method, Gradient Method, Separable, Quadratic, Chance-Constrained Linear Combinations & SUMT Programming Algorithms.

Text and Reference Books:

1. Operation Research By Taha – Pearson
2. Probability & Statistics with Reliability, Queuing & Computer Serine Application- Kishor S. Trivedi – Willey
4. Operation Research, K.Rajagopal – PHI
5. Operation Research Algorithms and Applications by Rathindra P.Sen, PHI

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
LIST OF EXPERIMENTS:

1. Design a CMOS inverter in schematic and simulate for Transient Characteristics.
2. Design a CMOS two input NAND gate, Two input NOR gate, Two input AND gate and Two input OR gate in schematic and simulate for Transient Characteristics.
3. Design the layout of a CMOS Inverter and simulate for DC (Transfer) and Transient characteristics.
4. Design the layout for two inputs NAND gate, two input OR gate, two input AND gate and two input NOR gate and simulate for DC (Transfer) and Transient characteristics.
5. Realized a two input EXOR gate in schematic, draw its layout and simulate for DC (Transfer) and Transient characteristics.
6. To realize a 1 bit full adder in CMOS schematic, design its layout using tool option and simulate for Transient Characteristics.
7. To realize a Boolean expression $Y=\text{Not} \left( (A+B)(C+D)E \right)$ in schematic, draw its layout and simulate for Transient Characteristics.
8. To realize a 4 X 1 MUX using transmission gates in schematic and simulate for Transient Characteristics.
9. To realize JK FLIPFLOP in CMOS schematic, design its layout and simulate for Transient Characteristics.
10. To Realize D FLIPFLOP and T FLIPFLOP in CMOS schematic, design its layout and simulate for Transient Characteristics.
11. To realize a four bit asynchronous counter using T flip-flop as a cell in schematic and simulate for Transient Characteristics.
12. To realize a four bit shift register using D flip-flop as a cell in schematic and simulate for Transient Characteristics.

NOTE:
7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTEC-505-B contents.
MTEC-537-B       ADVANCED MICROPROCESSORS & APPLICATIONS LAB

L     T     P     Credits
-----  -----  -----  
-      -      3      3

Class Work :  20 Marks
Exams      :  30 Marks
Total      :  50 Marks

(A few experiments may be designed & included in this list depending upon the infrastructure available in the institute)

1. To study the architecture of Microprocessor 8086 Kit
2. Write an ALP to convert a hexadecimal No. to decimal No. in single step execution  (DEBUG)
3. Write an ALP to enter a word from keyboard and to display
4. Write an ALP for addition of two one digit Numbers.
5. Write an ALP to display a string
6. Write an ALP reverse a string
7. Write an ALP to check whether the No. is Palindrome
8. To study the Microcontroller Kit
9. Write an ALP to generate 10 KHz frequency square wave
10. Write an ALP to generate 10 KHz & 100KHz frequency using interrupt
11. Write an ALP to interface intelligent LCD display
12. Write an ALP to interface intelligent LED display
13. Write an ALP to Switch ON alarm when Microcontroller receive interrupt
14. Write an ALP to interface one microcontroller with other using serial / parallel communication.

NOTE:
7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTEC-507-B contents.
MTEC-502-B ADVANCED ELECTRONICS INSTRUMENTATION

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Class Work : 25 Marks
Theory : 75 Marks
Total : 100 Marks
Duration of Exam. : 3 Hrs.

UNIT I

Digital instruments: A/D & D/A converters & their types, Data loggers, significance of 3 1/2 & 4 1/2 digit, automation in digital instruments, DMM, Digital frequency meter, universal counter & their applications.

UNIT II
Oscilloscopes & Signal Analyzers: Digital Storage oscilloscope & its features like Roll, Refresh & sampling rate, Application of DSO in communication, Sampling Oscilloscope, current trends in oscilloscope technology, Wave Analyzer & its Applications, FET analyzers & network analyzers; their applications.


UNIT III
Introduction to SCADA & PLC: Data acquisition system, evaluation of SCADA, communication technologies, monitoring and supervisory functions, Block diagram of PLC, programming languages, Ladder diagram, Functional block diagram, Applications, Interfacing of PLC with SCADA.

SCADA system components & Architecture: Schemes, Remote Terminal Unit, Intelligent Electronic Devices, Communication Network, SCADA server. Various SCADA Architectures: advantages and disadvantages of each system.

UNIT IV
PLC Programming: Instructions, operational procedures, PLC Registers: Characteristics of Registers, module addressing, holding registers, input registers, output registers. PLC Functions: Timer functions and Industrial applications, counters, counter function & industrial applications, Arithmetic functions, Number comparison functions, number conversion functions.

Virtual Instrumentation: Advantages, Block diagram & architecture of Virtual Instruments, Data Flow Techniques, graphical programming in data flow, development of virtual instruments using GUI, Real Time Systems.

Text and Reference Books:
1. Digital instrumentation, By Bouwens,A.J., MGH
2. Measuring systems-Application & Design, By Doebelin, MGH
3. Electronic measurements & instrumentation, by B. M. Oliver & J. M. Cage. MGH
4. SCADA supervisory control and data acquisition, by Stuart A Boyer

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I

Introduction to optical fiber: Introduction to ray theory, theory of optical wave propagation, optical fiber attenuation, optical fiber absorption, scattering and band losses, classification of optical fiber, dispersion, dispersion shifted fiber, dispersion modified fibers, dispersion compensated fibers, optical fiber non-linear effects.

Optical amplifier: Types of optical amplifier, Raman optical amplifiers, semiconductor optical amplifier, Erbium doped fiber amplifier, application: 155 Mb/s sonet/OC-3-stm transducer amplifier.

UNIT II

Optical transmitter and receiver: Introduction to multiplexer, 32:1 2.488 Gb/s multiplexer with clock generator (VSC 8131) external modulated laser diode, the effect of noise and power supply noise rejection, 10 Gb/s DWDM optical transmitter Introduction, Data pattern, photo detector diodes, classification of optical receiver, optical receiver performance characteristics.

Optical transceivers: Introduction, LED transceivers, LASER diode Trans receiver, design guide lines for optical channel transceivers, high speed optical channel transceivers.

UNIT III


Multiplexing: Introduction, WDM, future optical devices for DWDM schemes, DWDM multiplexing AWG multiplexer/demultiplexer for DWDM system add/drop multiplexer/demultiplexers, 2.5 Gb/s 16:1 multiplexer.

UNIT IV

Optical system: Introduction, optical power budget analysis, 10 Mb/s optical link designs for industrial applications, optical fiber link design, dispersion effect, wave polarization effect in optical systems under sea optical system, soliton transmission.

Network: Introduction, optical networks review of data communication links, networks, network transport architecture, LAN standards fiber channel asynchronous transfer mode, synchronous transfer mode.

Text Books:
1. Horal Kolimbris "fiber optical communication" Pearson

Reference Books:
2. Gerd Keiser, "Optical Fiber Communication", TMH

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In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I


UNIT II

Image Filtering in Frequency Domain, Wavelets and MultiResolution Processing

Filtering in Frequency Domain: Relationship between the sampling and frequency intervals, 2-D Impulse and shifting properties, 2-D Sampling & 2-D Sampling Theorem, Aliasing in Images, 2-D Discrete-Fourier Transform and its Inverse, Properties of 2-D DFT, Additional Characteristics & Filtering Fundamentals in the frequency domain, correspondence between filtering in the spatial and frequency domains; Smoothing frequency domain filters: Ideal Lowpass Filters, Butterworth Lowpass Filters, Gaussian Lowpass Filters; sharpening frequency domain filters: Ideal Highpass Filters, Butterworth Highpass Filters, Gaussian Highpass Filters, Laplacian in Frequency Domain; Unsharp Masking, Highboost Filtering, and High Frequency Emphasis Filtering, Homomorphic filtering. Implementation of DFT: computing 2-D DFT using 1-D DFT Algorithm, Computing IDFT using DFT Algorithm.


UNIT III

Image Restoration and Reconstruction

Restoration in presence of Noise only: A model of the image degradation/restoration process, Noise models: Spatial and frequency properties of noise, some important noise probability density functions, Periodic noise, Estimation of Noise Parameters; Restoration in the presence of noise spatial filtering: Mean Filters, Order Statistic Filters, Adaptive Filters; Periodic noise reduction by frequency domain filtering: Bandreject Filters, Bandpass Filters, Notch Filters


UNIT IV

Image Compression & Segmentation

Image Compression: Fundamentals: Coding Redundancy, Spatial and Temporal Redundancy, Irrelevant Information, measuring Image Information, Fidelity Criteria, Image Formats, Containers, and Compression Standards; Basic Compression Methods: Huffman Coding, Arithmetic Coding, LZW Coding, Run Length Coding, Symbol Based Coding, Bit Plane Coding, Block Transform Coding, Predictive Coding, Wavelet Coding, Digital Image Watermarking.


Text and Reference Books:

NOTE: In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
MTEC-534-B  ADVANCED OPTICAL COMMUNICATION LAB

L  T  P  Credits
-  -  3  3

Class Work : 20 Marks
Exams : 30 Marks
Total : 50 Marks

(A few experiments may be designed & included in this list depending upon the infrastructure available in the institute)

1. Study of optical devices.
2. Study of fiber optical detector.
3. Study of fiber optical transmitters
4. Determination of numerical aperture of optical fiber
5. Study of characteristics of LED.
6. Study of characteristics of LASER diode.
7. Setting a fiber optic analog link.
8. Setting a fiber optic digital link.
9. Study of modulation demodulation of light source by direct amplitude modulation techniques.
10. Forming a PC to PC communication link using optical fiber & RS 232.
11. Setting up a fiber optic voice link.
13. Study of modulation & Demodulation of light source by PWM technique.

NOTE:
7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTEC-504-B contents.
1. Take a hand written document, Perform pre-processing and try to segment into characters
2. Take an image, design fuzzy rules for content based image retrieval.
3. Take an image, design a neural network for content based image retrieval.
4. Write a program for image enhancement
5. Write a program for image compression
6. Write a program for color image processing
7. Write a program for image segmentation
8. Write a program for image morphology
9. Write a program for Image Restoration
10 Write a program for Edge detection
11. Write a program for Blurring 8 bit color versus monochrome

NOTE:
7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTEC-506-B contents.
UNIT I
CMOS Sub circuits: MOS Switch, MOS Diode, MOS Active Resistors, CMOS Regulated Cascade current source, Cascade current sink.

UNIT II
Current Mirrors: Passive and active current mirrors. Simple current mirror, Cascode current Mirror, Widlar current mirror, Wilson Current Mirror

UNIT III
Operational Amplifier: Applications of operational Amplifier, theory and Design, Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, gain boosting, two stage MOS operational Amplifier with cascades, MOS Folded-cascade operational amplifiers, noise in op-amps, op-amp stability and frequency compensation.
Comparators: Comparators Models and Performance, Development of a CMOS Comparator, Design of a Two-Stage CMOS Comparator, Other Types of Comparators.

UNIT IV
Nonlinear Analog Circuits:
Voltage controlled oscillator, Comparators, Source Follower Phase Locked Techniques; Phase Locked Loops (PLL), Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters.
OTA & Switched Capacitor filters:
OTA Amplifiers, Sampling Switches, Switched Capacitor Circuits and Switched Capacitor Filters OTA

Text Books:

Reference Books

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
MTEC-510-B  MULTIMEDIA COMMUNICATION

Class Work : 25 Marks
Theory : 75 Marks
Total : 100 Marks
Duration of Exam. : 3 Hrs.

UNIT I
Multimedia & Information Representation
Multimedia Introduction: multimedia networks, Telephone networks, Data networks, Broadcast television networks, Integrated services digital networks, Broadband multiservice networks, types of Multimedia Applications: Movie on Demand, Near Movie on Demand, communication modes, multipoint conferencing, network QOS, Application QOS.

UNIT II
Text and Image Compression
Compression Principles & Text Compression: Compression Principles: Source encoders and Destination decoders, Lossless and lossy compression, Entropy encoding, Source encoding; Text Compression: Static Huffman coding, Dynamic Huffman Coding, Arithmetic Coding.
Image Compression: Graphics Interchange Format, Tagged image file format, digitized documents, digitized pictures.

UNIT III
Audio and Video compression
Video compression: video compression principles, Motion Pictures Expert Group (MPEG), MPEG1, MPEG2.

UNIT IV
INTERNET AND DESIGNING FOR THE WORLD WIDE WEB

Text Books:
1. Fred Halsall, “Multimedia Communications”, Pearson
3. 

Reference Books

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I
Background: discrete-time signal processing, linear algebra, Mathematical preliminaries, Random variables & discrete-time random processes, Wiener filtering and MMSE estimates, Linear predication, Levinson-durbin algorithm and lattice, Classical detection and estimation theory, Statistical Models: Gaussian Distribution and relatives, Reproducing Distributions, Sample mean and variance, Fundamental of parametric and Linear Estimation,

UNIT II

UNIT III
Least Squares Algorithm: General Weighted Least Squares Methods, Recursive Least Squares Algorithm, Fast Least Squares Algorithm to AR modeling case

UNIT IV
Introduction to array processing, Composite Hypotheses in the Univariate Gaussian Model, Composite Hypotheses in the Multivariate Gaussian Model, Statistical Confidence Intervals,

Text and Reference Books:
1. Fundamentals of Statistical Signal Processing, Volume 1: Estimation Theory, Steven M. Kay
4. An Introduction to Statistical Signal Processing, Robert M. Grey, Lee D. Davisson

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I
Embedded Hardware And Software: Embedded system evolution trends, Terminology, Gates, Timing diagram, Memory, Microprocessor buses, Direct memory access, Interrupts, Built interrupts, Interrupts basis, Shared data problems, Interrupt latency, Interrupt routines in an RTOS environment.


UNIT II
Hardware/Software Co-Synthesis: The Co-Synthesis Problem, State-Transition Graph, Refined on and Controller Generation, Distributed System Co-Synthesis.

partitioning decision: Hardware / Software duality, coding Hardware, ASIC revolution, Managing the Risk, Co-verification, execution environment, memory organization, System start-up, Hardware manipulation, memory mapped access, speed and code density.

UNIT III

Interrupt Service Routines: Watch-dog timers, Flash Memory basic toolsset, Host based debugging, Remote debugging, ROM emulators, Logic analyser, Caches, Computer optimisation, Statistical profiling.

UNIT IV

In-Circuit Emulators & Testing: Buller proof run control, Real time trace, Hardware break points, Overlay memory, Timing constraints, Usage issues, Triggers, Bug tracking, reduction of risks & costs, Performance, Unit testing, Regression testing, Choosing test cases, Functional tests, Coverage tests, Testing embedded software, Performance testing, Maintenance.

Text and Reference Books:

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I

**Memory Interfacing:** Memory: Memory write ability and storage performance, Memory types, composing memory, Advance RAM interfacing communication basic.

**I/O INTERFACING:** Microprocessor interfacing I/O addressing, Interrupts, Direct memory access, Arbitration multilevel bus architecture, Serial protocol, Parallel protocols, Wireless protocols, Digital camera example.

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<td>Theory</td>
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UNIT II


UNIT III


**Embedded Ethernet:** Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT IV


**Text and Reference Books:**
2. Jan Axelson, ”Parallel Port Complete: Programming, interfacing and using the PC’s parallel printer port“, Penram publications, 1996.
3. Dogan Ibrahim, „Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series“, Elsevier 2008.

**NOTE:**
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
MTEC-518-B  SEMICONDUCTOR DEVICE MODELLING

Credits

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Class Work : 25 Marks  
Theory : 75 Marks  
Total : 100 Marks  
Duration of Exam. : 3 Hrs.

UNIT I

**Basic Semiconductor Physics:** Energy Bands and Charge Carriers, Band Model, Bond Model, MOS Capacitor, Hall Effect, MOSFET and Compound Semiconductor FET, MOSFET capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling

UNIT II

**Metal Semiconductor Junctions:** Equilibrium in Electronic Systems, Ideal metal semiconductor junctions, Schottky Barriers, Mott barrier, tunnel contacts and ohmic Contacts.  
**BJT:** Bipolar Junction Transistors, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors, Ebers-Moll Model, Hetero Junction Bipolar Transistor

UNIT III

**Noise modeling:** Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuits

**Other MOSFET models:** MOSFET Physical Effects, MOSFET High Field Effects, The BEV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, noise model temperature effects, MOS model 9, MOSAI model

UNIT IV

**Modeling of process variation and quality assurance:** Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests. Recent Developments in Microelectronic Devices.

Text and Reference Books:
3. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, *Device Modeling for Analog and RF CMOS Circuit Design*, John Wiley & Sons Ltd.

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
ADVANCE SATELLITE COMMUNICATION

UNIT I

Multiple Access: FDMA, TDMA, CDMA, SSMA- comparison of multiple access techniques, Practical Demand Access systems, Multiple Access With on board processing.

UNIT II

Overview of GPS: Basic concept, system architecture, space segment, user segment, GPS aided Geo-augmented navigation (GAGAN) architecture. GPS Signals: Signal structure, anti spoofing (AS), selective availability, Difference between GPS and GALILEO satellite construction.

UNIT III
GPS orbits and satellite position determination : GPS orbital parameters, description of receiver independent exchange format (RINEX) – Observation data and navigation message data parameters, GPS position determination.
GPS Errors : GPS error sources – clock error, ionospheric error, tropospheric error, multipath, ionospheric error estimation using dual frequency GPS receiver.

UNIT IV

Phased Arrays in Radar and Communication Systems: System requirements for radar and communication antennas, Array characterization for radar and communication systems, Fundamental results from array theory, Array size determination.

Text Books:
1. T. Pratt and C.W., -- Bostian Satellite Communications.
2. Tri T. Ha, --Digital Satellite Communication (2 ed) 3 Robert J. Mailloux

Reference Books:
3. Dr. D.C. Agarwal, -- Satellite Communication.

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I
A Beginning with some practical situations, which call for multiresolution/multiscale analysis - and how time-frequency analysis and wavelets arise from them. Examples: Image Compression, Wideband Correlation Processing, Magnetic Resonance Imaging, Digital Communication.
Piecewise constant approximation - the Haar wavelet, Building up the concept of dyadic Multiresolution Analysis (MRA). Relating dyadic MRA to filter banks, A review of discrete signal processing, Elements of multirate systems and two-band filter bank design for dyadic wavelets.
UNIT II
Families of wavelets: Orthogonal and biorthogonal wavelets, Daubechies’ family of wavelets in detail. Vanishing moments and regularity, Conjugate Quadrature Filter Banks (CQF) and their design, Dyadic MRA more formally, Data compression - fingerprint compression standards, JPEG-2000 standards.
UNIT III
Journey from the CWT to the DWT: Discretization in steps, Discretization of scale - generalized filter bank, Discretization of translation - generalized output sampling, Discretization of time/ space (independent variable) - sampled inputs.
Going from piecewise linear to piecewise polynomial, The class of spline wavelets - a case for infinite impulse response (IIR) filter banks.
UNIT IV
An exploration of applications (this will be a joint effort between the instructor and the class). Examples: Transient analysis; singularity detection; Biomedical signal processing applications; Geophysical signal analysis applications; Efficient signal design and realization: wavelet based modulation and demodulation; Applications in mathematical approximation; Applications to the solution of some differential equations; Applications in computer graphics and computer vision; Relation to the ideas of fractals and fractal phenomena.

Text and Reference Books:
2. E. Mallat.. A Wavelet Tour of Signal Processing, Elsevier, Indian Ed.
4. G. Kaiser.. A Friendly guide to Wavelets, Birkhauser

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
MTEC-524-B

DSP PROCESSORS

L T P Credits
4 - - 4

Class Work : 25 Marks
Theory : 75 Marks
Total : 100 Marks
Duration of Exam. : 3 Hrs.

UNIT I

Introduction To DSP Processors: Advantages of DSP, characteristics of DSP systems, classes of DSP applications, DSP processor embodiment and alternatives, Fixed Vs Floating point processors, fixed point and Floating point Data Paths.

DSP Architecture: An introduction to Harvard Architecture, Differentiation between Von-Neumann and Harvard Architecture, Quantization and finite word length effects, Bus Structure, Central Processing Unit, ALU, Accumulators, Barrel Shifters, MAC unit, compare, select, and store unit (CSSU), data addressing and program memory addressing.

UNIT II

Memory Architecture: Memory structures, features for reducing memory access required, wait states, external memory interfaces, memory mapping, data memory, program memory and I/O memory, memory mapped registers.

Addressing & Instruction Set: Various addressing modes - implied addressing, immediate data addressing, memory direct addressing, register direct and indirect addressing, and short addressing modes, Instruction types, various types registers, orthogonality, assembly language and application development.

UNIT III

Execution Control And Pipelining: Hardware looping, interrupts, stacks, pipelining and performance, pipelining depth, interlocking, branching effects, interrupt effects, instruction pipelining.

PERIPHERALS: Serial ports, timers, parallel ports, bit I/O port, host ports, communication ports, on-chip A/D and D/A converters, external interrupts, on chip debugging facilities, power consumption and management.

UNIT IV

Processors: Architecture and instruction set of TMS320C3X, TMS320C5X, TMS320C6X, ADSP 21XX DSP Chips, some example programs.

Recent Trends In DSP System Design: FPGA-based DSP System Design, advanced development tools for FPGA, Development tools for Programmable DSPs, Code Composer Studio.

Text and Reference Books:


NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
MTEC-526-B

COMMUNICATION NETWORK

Class Work : 25 Marks
Theory : 75 Marks
Total : 100 Marks
Duration of Exam. : 3 Hrs.

UNIT I
Propagation path-loss models: Mechanism, free space path loss, log-distance path loss models, Okumara model, Hata model, PCS model, Wideband PCS microcell model, indoor propagation models, Jake’s channel model, Multi path characteristics of radio waves, signal fading, Time dispersion, Doppler spread, coherence time LCR, fading statistics, diversity techniques.

UNIT II
Wireless systems and standards: GSM standards, signaling and call control, mobility management, location tracing, wireless data networking, packet error modeling on fading channels, wireless data services, IS-95, GPRS.
Mobile Network Layer: Mobile IP (Goals, assumptions, entities and terminology, IP packet delivery, agent advertisement and discovery, registration, tunneling and encapsulation, optimizations), Dynamic Host Configuration Protocol (DHCP).

UNIT III
Data Dissemination: Communications asymmetry, classification of new data delivery mechanisms, pushbased mechanisms, pull-based mechanisms, hybrid mechanisms, selective tuning (indexing) techniques.
Network Operating Systems: Overview of network operating systems (Windows NT/Unix/Linux), Mobile IP3SN Operating System.

UNIT IV
Mobile Ad hoc Networks (MANETs): Overview, Properties of a MANET, spectrum of MANET applications, routing and various routing algorithms, security in MANETs.
Vehicular Ad Hoc Networks (VANETs): VANET architecture, Basic principles and applications of VANETs, Information dissemination in VANETs, brief introduction to vehicular mobility modeling for VANETs, challenges in VANETs, difference between VANETs and MANETs, overview of controller area network (CAN), DSRC (dedicated short range communications),Routing Protocols in Vehicular Ad Hoc Networks, optimization algorithm (PSO).

Text Books:
2. Mobile communications by Jochen H. Schiller, Wesley
3. VANET: Vehicular Applications and Inter-Networking Technologies by Hannes Hartenstein, Kenneth Laberteaux, john willey and sons
4. Advances in Vehicular Ad-Hoc Networks: Developments and Challenges by Mohamed Watfa, IGI Global

Reference Books:
2. Data communications and networking by Forouzan

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I

UNIT II

UNIT III
CDMA as a protocol – Multiple Access Techniques: classification of multiple access protocols – contention less (scheduling) multiple access protocols – contention (random) multiple access protocols – Code division multiple access (CDMA) protocols – CDMA system concepts – spread spectrum multiple access – Code generation – DSCDMA with imperfect power control – Near – far effect – multi user interference in the reverse link and forward link.

UNIT IV
Advanced Intelligent Networks: Introduction, Advanced Intelligent Networks (AIN), Intelligent Networking (IN), SS7 Protocol (Signaling System # 7), Component Used in IN/AIN Architecture, Working of AIN, Difference Between IN and Succeeding AIN/IN, Intelligent Cell Concept, Zone Divided Power Delivery Intelligent Cells, Processing Gain Intelligent Cells, Applications of Intelligent Cell Concept, Advantages of Intelligent Cells Implementation

Text Books:
3. Mobile Communication: Jochen Schiller Pearson Education.

Reference Books:
2. Kamilo Feher: Wireless Digital communications, Modulation and Spread S

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I
Introduction: Study of reliability and maintainability, concepts terms and definition, random events, bayes' formula, random variables, discrete distribution, binomial distribution, Poisson distribution, continuous distribution
Basic Reliability model: Reliability function, mean time to failure, hazards rate function, bath tub, conditional reliability, constant failure rate model, time dependent failure model.

UNIT II
Data collection and empirical method: Data collection, Empirical Method, Ungrouped complete data, grouped complete data, ungrouped censored data, group censored data, static life estimation
Reliability Testing: product testing, reliability life testing, test time calculation, length of test, burn in testing, acceptance testing, experimental design, reliability growth process, idealized growth curve, Duane Growth Model, AMSAA Model.

UNIT III
Failure and Repair Distribution: candidate distribution, probability plots and least square curve fitting, parameter estimation, confidence intervals, parameter estimation for covariance model.
Goodness to fit test: Chi Square Goodness Of fit test, Basletts test for exponential distribution, Mann's Test for Weibull Distribution, Kolmogosov Smirnov test for normal, Log normal Distribution, Test for Power Law process model, On fitting distribution.

UNIT IV
Reliability Estimation and Applications: Redundancy, burn in testing, preventive main furnace analysis, Reliability Allocation, Reliability growth testing, Repairable system analysis, multiply censored data.
Implementation: Objectives function and processes the economics of reliability and maintain ability and system design organisational consideration, data source and data collection methods, product reliability, warranties & related matters, Software Reliability.

Text Books:
1. Reliability and Maintain Ability Engineering. Charles E. Ebeling TMH.

Reference Books

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
MTEC-631-B  ADVANCED WIRELESS COMMUNICATION SYSTEM LAB

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Class Work : 20 Marks
Exams : 30 Marks
Total : 50 Marks

LIST OF EXPERIMENTS:

1. Frequency Offset Estimation and Correction
3. Antenna Resonance and Gain Bandwidth measurement
4. Characterization of Fading Effects
5. Fading Counter-measures using Antenna diversity and Frequency diversity
6. Delay Spread Measurement
7. Handover Demonstration
8. Detailed receiver and transmitter parameters of a typical radio communication system – SINAD, fidelity, image rejection, modulation sensitivity, transmission bandwidth etc.
9. PC2PC communication – protocol standards, frame/packet/UDP structure etc
10. Multiple channel DSSS – spreading, despreading, decoding etc.
11. Horn, micro strip antenna – radiation pattern, gain etc.
14. OFDM Synchronization, Frequency Offset, and Channel Estimation.
15. OFDM Modulator and Demodulator

NOTE:
7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTEC-601-B contents.
CMOS MIXED SIGNAL CIRCUIT DESIGN

L T P Credits
4 - 4 4

Class Work : 25 Marks
Theory : 75 Marks
Total : 100 Marks
Duration of Exam. : 3 Hrs.

UNIT I
PLL: Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL.
Switched Capacitor Circuits: Switched Capacitor circuits - basic principles, some practical circuits such as switched capacitor integrator, biquad circuit, switched capacitor filter, switched capacitor amplifier, non-filtering applications of switched capacitor circuit such as programmable gate arrays, DAC and ADC, MOS comparators, modulators, rectifiers, detectors, oscillators.

UNIT II
Sampling Circuits: Sampling circuits: Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures: Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.
DAC: Input/output characteristics of an ideal D/A converter, performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, switching functions to generate an analog output corresponding to a digital input. D/A converter architectures: Resistor-Ladder architectures, current-steering architectures.

UNIT III
Filters: Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-C integrator, discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transfer function.

UNIT IV
Data Converter Snr: Quantization Noise, Signal to Noise Ratio, improving SNR by using Averaging and Feedback.
Mixed-Signal Layout Issues: Floor planning, Power Supply and Ground Issues, Fully Differential Design, Guard Rings, Shielding, Other Interconnect Considerations

Text and Reference Books:
2. Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I
MEMS and Microsystems: Overview of CMOS process in IC fabrication, MEMS system-level design methodology, Microfabrication Evolution, Microsystems miniaturization, Microsystem Applications in health care industry, aerospace industry, telecommunications.

Microsensors and Microactuation: Working principles of Microsystems, Microsensors - acoustic wave sensors, biomedical sensors, optical sensors, thermal sensors, Pressure sensors with embedded electronics (Analog/Mixed signal); Accelerometer with transducer, Gyroscope, RF MEMS, optical MEMS, Sensor noise calculation, Bolometer Design, Microactuation overview, Microactuation using thermal forces, electrostatic forces, shaped memory alloys, piezoelectric crystals, Micogrippers, Micromotors, Microvalves, Micropumps, Microaccelerometers, Microfluidics.

UNIT II

Microsystem Design-Thermofluid Engineering: Thermofluid engineering and microsystem design - fluid mechanics at macro and meso scale, fluid flow in nanoscale designs.

UNIT III
Scaling laws in Miniaturized Designs: Scaling in electrostatic forces, electromagnetic forces, Scaling in electricity, fluid mechanics and heat transfer.

Microsystems fabrication processes: Materials for MEMS and Microsystems, Photolithography, Ion Implantation, Diffusion, CVD, PVD, Epitaxy, Etching with reference to concerns involved in microfabrication.

UNIT IV
Micromanufacturing: Bulk Micromanufacturing, Surface Micromachining, LIGA Process

Micropackaging: Microsystem Packaging, Interfaces in Microsystem Packaging, Packaging Technologies, Three dimensional packaging, Microsystems assembly, Selection of Packaging Materials

Text Books:

Reference Books:
2. Ljubisa Ristic, Editor, Sensor Technology and Devices, Artech House, 1994

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
MTEC-609-B  ALGORITHM FOR VLSI DESIGN

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Class Work : 25 Marks
Theory : 75 Marks
Total : 100 Marks
Duration of Exam. : 3 Hrs.

UNIT I

Logic synthesis & verification:
Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

Partitioning: problem formulation, cost function and constraints, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

UNIT II

Floor planning & pin assignment: Floor planning model and cost function, Classification of Floor planning, constraint based floor planning, Integer Programming Based Floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

Placement: problem formulation, cost function and constraints, simulation base placement algorithms, Partitioning Based Placement Algorithms, other placement algorithms.

UNIT III

Global Routing: Grid Routing and Global routing, Problem formulation, cost function and constraints, classification of global routing algorithms, routing regions, sequential global routing, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, Integer Programming Based Approach, Hierarchical Global Routing, Global Routing by Simulated Annealing

Detailed routing: problem formulation, cost function and constraints, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

UNIT IV

Over the cell routing & via minimization: Over-the-cell Routing: Cell Models, two layers over the cell routers, Three-Layer Over-the-cell Routing, constrained & unconstrained via minimization.

Compaction: problem formulation, Classification of Compaction Algorithms one-dimensional compaction, two dimension based compaction, hierarchical compaction

Text and Reference Books:

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I

EMBEDDED LINUX, WIN C.

UNIT II

TINY OS:

UNIT III

Overview Of RTOS 9: RTOS Task and Task state - Process Synchronization - Message queues - Mail boxes - pipes - Critical section - Semaphores - Classical synchronization problem - Deadlocks
Real Time Models And Languages: Event Based - Process Based and Graph based Models - Real Time Languages - RTOS Tasks - RT scheduling - Interrupt processing - Synchronization - Control Blocks - Memory Requirements.

UNIT IV

Real Time Kernel: Principles - Design issues - Polled Loop Systems - RTOS Porting to a Target - Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

Text and Reference Books:

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
UNIT I


Software For Embedded System Design: Development tools/ environments, Assembly language programming style, Interpreters, High level languages, Intel hex format object files, Debugging.

UNIT II

AVR Microcontroller: Introduction to AVR microcontroller, features of AVR family microcontrollers, different types of AVR microcontroller, architecture, memory access and instruction execution, pipelining, program memory considerations, addressing modes, CPU registers, instruction set, and simple operations.


UNIT III


ARM Programming: The ARM Programmer’s model, ARM Development tools, ARM Assembly Language Programming and C-compiler programming.

UNIT IV


Text and Reference Books:


NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.
MTEC-633-B  SEMINAR

L    T     P    Credits
-  -  2      2

Class Work :  50 Marks
Exams     :  --
Total     :  50 Marks

The objectives of the course remain:
- To learn how to carry out literature search
- To learn the art of technical report writing
- To learn the art of verbal communication with the help of modern presentation techniques

A student will select a topic in emerging areas of Engineering & Technology and will carry out the task under the supervision of a teacher assigned by the department.

He/She will give a seminar talk on the same before a committee constituted by the chairperson the department. The committee should comprise of 2 or 3 faculty members from different specializations. The teacher(s) associated in the committee will each be assigned 2 hours teaching load per week.

However, supervision of seminar topic will be in addition to the regular teaching load.
The primary objective of this course is to develop in student the capacity for analysis & judgment and the ability to carry out independent investigation in design/development through a dissertation work involving creativity, innovation and ingenuity. The work must start with comprehensive literature search and critical appreciation thereof so as to select research problem the student wishes to work on.

Each student will carry out independent dissertation under the supervision of some teacher(s) who will be called Supervisor(s). In no case more than two supervisors can be associated with one dissertation work. The dissertation involving design/ fabrication/ testing/ computer simulation/ case studies etc. which commences in the III Semester will be completed in IV Semester. The evaluation of the dissertation phase - I besides approval of the dissertation topic of the students will be done by a committee constituted as under:

- Chairperson of Department: Chairperson
- M Tech Coordinator/ Sr Faculty: Member Secretary
- Respective dissertation supervisor: Member

The student will be required to submit two copies of his/her report to the department for record (one copy each for the department and participating teacher).
The dissertation started in III Semester will be completed in IV Semester and will be evaluated in the following manner.

Internal Assessment

Internal Assessment (class work evaluation) will be effected as per ordinance through interim report, presentation and discussion thereon by the following committee of three persons:

- Chairperson of Department: Chairperson
- M Tech Coordinator/ Sr Faculty: Member Secretary
- Respective dissertation supervisor: Member

External Assessment

Final dissertation will be assessed by a panel of examiners consisting of the following:

- Chairperson of Department: Chairperson
- Respective Supervisor(s): Member(s)
- External expert: To be appointed by the University

NOTE: The External Expert must be from the respective area of specialization. The chairperson & M Tech Coordinator with mutual consultation will divide the submitted dissertations into groups depending upon the area of specialization and will recommend the list of experts for each group separately to the V C for selecting the examiners with the note that an external expert should be assigned a maximum of FIVE dissertations for evaluation.

The student will be required to submit THREE copies of his/her report to the M Tech Coordinator for record and processing.