SCHEME & SYLLABUS OF M.TECH ECE EFFECTIVE FROM 2012-13

DEENBANDHU CHHOTU RAM UNIVERSITY OF SCIENCE & TECHNOLOGY, MURTHAL (SONEPAT)

SCHEME OF STUDIES & EXAMINATION FOR

MASTER OF TECHNOLOGY DEGREE COURSE IN
ELECTRONICS & COMMUNICATION ENGINEERING
(Credit Based Scheme w.e.f 2012-13)

SEMESTER I

Sr.No	Course No.	Course Title	Teaching Schedule		Marks of Class Work	Exam. Marks		Total Marks	Credit	Duration of Exam.
			L	P		Theory	Practical			
1	MTEC-501-B	Advanced Digital Signal Processing	4	-	25	75	-	100	4	3
2	MTEC-503-B	Information & Communication Theory	4	-	25	75	-	100	4	3
3	MTEC-505-B	Digital VLSI design	4	-	25	75	-	100	4	3
4	MTEC-507-B	Advance Microprocessor & Application	4	-	25	75	-	100	4	3
5	MTEC-509-B	Optimization Techniques	4	-	25	75	-	100	4	3
6	MTEC-531-B	Digital VLSI Design Lab	-	3	20		30	50	1.5	3
7	MTEC-537-B	Advance Microprocessors & Applications Lab	-	3	20		30	50	1.5	3
Total			**20**	**6**	**165**	**375**	**60**	**600**	**23**	

Note:

1. The students will be allowed to use non-Programmable Scientific Calculator. However, sharing/exchange of calculator are prohibited in the examination.
2. Electronics Gadgets including Cellular Phones are not allowed in the examination.

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SEMESTER II

Sr.No	Course No.	Course Title	Teaching Schedule		Marks of Class Work	Exam. Marks		Total Marks	Credit	Duration of Exam.
			L	P		Theory	Practical			
1	MTEC-502-B	Advanced Electronics Instrumentation	4	-	25	75	-	100	4	3
2	MTEC-504-B	Advanced Optical Communication	4	-	25	75	-	100	4	3
3	MTEC-506-B	Digital Image Processing	4	-	25	75	-	100	4	3
4		Elective-1	4	-	25	75	-	100	4	3
5		Elective-II	4	-	25	75	-	100	4	3
6	MTEC-534-B	Advanced Optical communication lab	-	3	20		30	50	1.5	3
7	MTEC-536-B	Advanced image Processing Lab	-	3	20		30	50	1.5	3
Total			**20**	**6**	**165**	**375**	**60**	**600**	**23**	

ELECTIVE – I		**ELECTIVE - II**	
MTEC-508-B	Analog VLSI Design	MTEC-518-B	Semiconductor Device Modeling
MTEC-510-B	Multimedia Communication	MTEC-520-B	Advanced Satellite Communication
MTEC-512-B	Statistical Signal Processing	MTEC-522-B	Multirate and Wavelet signal Processing
MTEC-514-B	Design of Embedded system	MTEC-524- B	DSP Processor
MTEC-516-B	Embedded Networking	MTEC-526-B	Communication Network

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SEMESTER III

Sr.No	Course No.	Course Title	Teaching Schedule		Marks of Class Work	Exam. Marks		Total Marks	Credit	Duration of Exam.
			L	P		Theory	Practical			
1	MTEC-601-B	Advanced Wireless Communication System	4	-	25	75	-	100	4	3
2	MTEC-603-B	Reliability Engineering	4	-	25	75	-	100	4	3
3		Elective-III	4	-	25	75	-	100	4	3
4	MTEC-631-B	Advance Wireless Communication Lab		3	20		30	50	1.5	3
5	MTEC-633-B	Seminar	-	2	50	-	-	50	2	-
6	MTEC-635-B	Project	-	3	20		30	50	1.5	-
7	MTEC-637-B	Dissertation (Phase-I)	-	6	100	-		100	6	-
Total			**12**	**14**	**265**	**225**	**60**	**550**	**23**	**-**

ELECTIVE 3	
MTEC-605-B	CMOS Mixed signal circuit design
MTEC-607-B	MEMS and IC Integration
MTEC-609-B	Algorithm for VLSI Deign
MTEC-611-B	Software for Embedded System
MTEC-613-B	Embedded Application Based on Advance Microcontroller

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SCHEME OF STUDIES & EXAMINATION FOR

MASTER OF TECHNOLOGY DEGREE COURSE IN
ELECTRONICS & COMMUNICATION ENGINEERING
(Credit Based Scheme w.e.f 2013-14)

SEMESTER IV

Sr.No	Course No.	Course Title	Teaching Schedule		Marks of Class Work	Exam. Marks		Total Marks	Credit
			L	P		Theory	Practical		
1	MTEC-602-B	**Dissertation**	-	20	50	-	100	150	20
Total				**20**	**50**	**-**	**100**	**150**	**20**

NOTE:

1. The students will be allowed to use non-Programmable Scientific Calculator. However , sharing/exchange of calculator are prohibited in the examination.
2. Electronics Gadgets including Cellular Phones are not allowed in the examination.

MTEC-501-B ADVANCED DIGITAL SIGNAL PROCESSING

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Sampling and Multi rate Digital Signal Processing:

Sampling: Review of Basic Sampling theorem, Sampling for Band limited Signals with sampling rate less than twice of maximum frequency, integer band positioning, Arbitrary band Positioning, Reconstruction, sampling rate conversion.

Multi rate Signal Processing (MSP): Need for MSP, Increasing & Decreasing sampling rate by integer factor (Interpolation & Decimation), Changing the sampling rate by rational factor, Structures for sampling rate conversion: Polyphase Filter implementation, cascaded integrator comb Filters; Multistage Structures, Applications of MSP.

UNIT II

Linear Prediction & Optimum Linear Filters:

Random Process, Stationary Random Process, Statistical/Ensemble Averages, Ensemble Averages for joint Random Processes, Power Density Spectrum, Discrete –Time Random Signals, Time-Averages for a discrete-time Random Process, Mean Ergodicity, Correlation Ergodic Process.

Stationary Random Process Representation: AR, MA & ARMA Processes, autocorrelation sequence and filter coefficients association; Linear Prediction: Backward & Forward; Optimum Reflection coefficients for lattice backward & forward predictors, AR process and linear prediction Relationship.

UNIT III

Power Spectrum Estimation:

Nonparametric methods: Spectra Estimation from finite duration Observations of signals: Energy Density Spectrum, Autocorrelation and power spectrum of Random signals: The Periodogram; Use of DFT in Power Spectrum Estimation; Nonparametric methods: Bartlett Method, The Welch Method, Blackman & Tukey method, Performance characteristics of Nonparametric power spectrum estimators, Computational Requirements of Nonparametric Power Spectrum Estimates.

Parametric methods: Relationship between Autocorrelation and the Model parameters, Yule-Walker method for AR Model Parameters, Burg method for AR model parameters, Unconstrained Least Squares method for AR model parameters, Sequential Estimation methods for the AR Model parameters, AR Model order selection, MA model for Power Spectrum Estimation, ARMA Model for Power spectrum Estimation.

UNIT IV

Finite word length effects and DSP applications:

Finite word length effects in Digital Filters: Number Representation Systems: Binary, Fixed Point Arithmetic, Floating Point Arithmetic, Number Quantization, Error due to coefficient Quantization, Low Sensitive Realizations, Quantization of product, Signal Scaling, Output Round off Noise Minimization, Limit Cycle Oscillations.

Applications of DSP: Applications to Speech Processing: Model of Speech production, Short-Time Spectrum Analysis, Speech processing system, Homomorphic Processing of speech; Hilbert Transformers, Adaptive Digital Filters: Wiener Filter, Newton Algorithm, Steepest –Descent Algorithm, Least Mean Square Algorithm, Recursive Filters, Applications of Adaptive Filters.

Text Books:

1. J. G. Proakis, D. G. Manolakis, "Digital Signal Processing, Principles, Algorithms, & Applications", Prentice –Hall India.
2. L. R. Rabiner & B. Gold, "Theory and Application of Digital Signal Processing", Prentice –Hall India.

Reference Books:

3. Andreas Antoniou, "Digital Signal Processing, Signals, Systems, and Filters", Tata McGraw –Hill\
4. V. Oppenheim, R. W. Schafer, J. R. Buck, "Discrete –Time Signal Processing", Prentice –Hall India.
5. V. Oppenheim, R. W. Schafer, "Digital Signal Processing", Prentice –Hall India.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-503-B INFORMATION AND COMMUNICATION THEORY

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Field Algebra: Introduction, Binary operations, Groups, Characteristics of the field, Binary field arithmetic, Galois field, vector spaces, matrices.

Block Codes: Linear block codes, The Generator & parity check matrices, Syndrome decoding, Hamming codes, BCH codes, Reed Solomon codes, Justeen codes, MDS code, Reed Muller Code.

UNIT II

Channel Coding: Waveform Coding, types of error control, structured sequences, error detecting and correcting capability, usefulness of standard array, cyclic codes, interleaving and concatenated codes, coding and interleaving applied to the compact disc, turbo codes.

Source Coding: Sources, amplitude quantizing, adaptive prediction, transform coding, source coding for digital data, examples of source coding.

UNIT III

Modulation and coding tradeoffs : Goals of communication system designer, error probability plane, Nyquist minimum bandwidth, Shannon Hartley capacity theorem, bandwidth efficiency plane, modulation and coding tradeoffs, designing and evaluating digital communication systems, bandwidth efficient modulation, modulation and coding for band limited channels, trellis coded modulation

Performance of codes: Performance of linear block codes & convolution codes, Bounds on code performance, Bounds on error performance.

UNIT IV

Estimation and Hypothesis Testing: Time and Ensemble Averages, Covariance and Correction Functions. Simple binary hypothesis tests, Decision Criteria, Neyman Pearson tests, Bayes Criteria, Multiple Hypothesis testing, Composite hypothesis testing, Asymptotic Error rate of LRT for simple hypothesis testing.

Properties of Estimators and filtering: Unbiasedness, efficiency, C-R bound, asymptotic properties, Wiener filter, Kalman filter.

Text Books:

1. Bernard Skylark & Pabitra Kumar Ray, Digital communications Fundamentals and Applications, Pearson
2. J. Das., S.K. Mullik & P.K. Chatterjee, Principles of digitals communication, New Age International Publishers
3. Papoulis, Athanasios, Probability Random Variables and Stochastic Processes, McGraw-Hill (2008).
4. Taub Schilling, Principles of Communication Systems
5. Harry L Vantrees, Detection ,Estimation and modulation Theory A Willey Interscience Publication

Reference Books:

1. Statistical Signal Processing – Detection, Estimation and Time-Series Analysis, Louis L. Scharf, Addison-Wesley 1991, ISBN 0-201-19038-9.
2. Probability, Random Processes, & Estimation Theory for Engineers, 3rd Edition, H. Stark & J. W. Woods, 2002.
3. An Introduction to Signal Detection and Estimation, Vincent Poor, 2nd ed., 1991
4. L. Scharf, Statistical Signal Processing - Detection, Estimation and Time Series Analysis, Addison-Wesley, 1991.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-505-B DIGITAL VLSI DESIGN

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Introduction: VLSI Design flow, Design hierarchy, VLSI design style, computer - Aided Design Technology, Basic principle of MOS transistor, Introduction to large signal MOS models for digital design, geometric scaling theory, small device models and effects. **The MOS Inverter:** Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Latch-up, Propagation Delay and Power Consumption.

UNIT II

Symbolic and Physical Layout Systems: MOS Layers Stick/Layout Diagrams, Layout Design Rules, Transistor layout, Inverter layout, CMOS digital circuit layout Issues of Scaling, Scaling factor for device parameters.
Performance Estimation: Resistance Estimation, Capacitance Estimation, Inductance Estimation, Switching characteristics, CMOS-gate transistor Sizing,

UNIT III

Combinational Logic Structures: CMOS Logic Families - static, dynamic and differential logic families, CMOS Complimentary logic, Pseudo NMOS logic, Dynamic CMOS logic, CMOS Domino logic, Clocked CMOS logic, pass Transistor logic, transmission gates logic circuits, complimentary switch logic.
Sequential Logic Design: SR latches, Flip flops: JK, D, Master- Slave & Edge triggered. Registers, CMOS Schmitt trigger.

UNIT IV

Subsystem Design: Design of an ALU Subsystem: design 4-bit simple and carry look ahead adder, multiplier design: serial-parallel multiplier, Braun Array, Wallace tree Multiplier, Design of 4-bit Shifter.
Low Power CMOS Logic: overview of power consumption, Low power design: Voltage Scaling, optimization of switching activity

Text Books:

1. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, "Digital Integrated Circuits" Second Edition, PH/Pearson, 2003.
2. D. A. Pucknell and K. Eshraghian, "Basic VLSI Design", Third Edition, PHI, 1994.
3. S. M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits : Analysis and Design", Third Edition, MH, 2002

Reference Books:

1. W. Wolf, Modern VLSI Design: System on Chip, Third Edition, PH/Pearson, 2002.
2. N. Weste, K. Eshraghian and M. J. S. Smith, *Principles of CMOS VLSI Design*" Pearson, 2001.
3. John P.Uyemura, CMOS Logic Circuit Design

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-507-B ADVANCED MICROPROCESSORS & APPLICATIONS

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

DESIGN OF MICROPROCESSOR: Design of basic microprocessor architectural Concepts: Microprocessor architecture, word Lengths, addressable memory, and Microprocessor's speed architectural characteristics, registers, instruction, memory addressing architecture, ALU, GPR's Control logic & internal data bus.

MICROPROCESSOR INSTRUCTIONS & COMMUNICATION: Instruction Set, Mnemonics, Basic Instruction Types, Addressing modes, Microprocessor I/O connecting I/O put to Microprocessor, Polling and Interrupts, Interrupt and DM. Controllers.

UNIT II

ADVANCED MICROPROCESSOR: Advanced microprocessors: Intel X86 family of advanced Microprocessor, programming model of 86 families, X86 addressing modes, instruction set, hardware.

HIGH PERFORMANCE CISC ARCHITECTURE (PENTIUM): The software model, functional description, CPU pin descriptions, RISC concepts, bus operations, super scalar architecture, pipe-lining, Branch prediction.

UNITIII

PENTIUM PROCESSOR: The instruction and caches, Floating point unit, protected mode operation, Segmentation, paging, multitasking, Exception and interrupts, Input / Output, Virtual 8086 model, Interrupt processing,

INSTRUCTIONS & PROGRAMMING WITH PENTIUM PROCESSOR: Instruction types, Addressing modes, Processor flags, Instruction set, Basic programming the Pentium Processor.

UNIT IV

PENTIUM PROCESSOR I/O: Data Communication, parallel I/O serial communication, Serial interface and UART modems, I/O devices, D/A, A/D interface, special I/O devices.

DEVELOPING PENTIUM PROCESSOR BASED APPLICATIONS: Introduction to the Design Process, Preparing the specifications, Developing a design, Implementing and Testing and design, Regulatory Compliance Testing, design tool for Development.

Text and Reference Books:

1. "The Intel Microprocessors 8086- Pentium Processor", Brey, 4th Edition, 2005.
2. "Microprocessors and Interfacing", D.V. Hall, TMH, 2nd Edition, 2006.
3. "Microcomputer Systems: The 8086/8088 Family: Architecture, Programming and Design", Liu Yu-Chang and Gibson Glenn A., PHI, 2003.
4. "Advanced Microprocessors and Peripherals Architectutes, Programming and Interfacing", Ray A.K. and Bhurchandi, TMH, 2002.
5. "Microprocessor based system design UBS", Rafiquzzman, Wiley-Interscience, 5th Edition, 2005.
6. "The X86 PC: Assembly Language, Design and Interfacing", M.A. Mazidi, J.P. Mazidi and Danny Causey, Peason, 5th Edition, 2011.
7. "The X86 Microprocessor(Architecture, Programming and Interfacing)", L.B. Das, Pearson, 2010.
8. "Advanced Microprocessor", Daniel Tabak, TMH, 2nd Edition, 2012.
9. "Fundamentals of Microprocessor and Microcomputers", B.Ram, Dhanpat Rai Publications, 5th Edition, 2008.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-509-B OPTIMIZATION TECHNIQUES

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Introduction: Operation Research Models, OR Model, Queuing & Simulation Models, Two Variable LP Model, Graphical LP solution, Computer Solution with solver & AMPL, Linear Programming Applications.

Sensitivity & Post Optimal Analysis: LP Model in Equation Form, Algebraic Solution, Simplex Method, Artificial Starting Solution, Sensitivity Analysis, Dual Problem, Primal-Dual Relationships, Economic Interpretation of Duality, Additional Simplex Algorithms, Post Optimal Analysis.

UNIT II

Models: Transportation Models and its variants, Transportation Algorithms, Assignment Models, Shortest Route Problem and its Algorithms, Maximal Flow Model, CPM & PERT.

Programming: Simplex Method Fundamentals, Bounded Variables Algorithms, Parametric Linear Programming, Goal Programming Algorithms, Integer Linear Programming & Algorithms, Heuristic Programming, Greedy Heuristics, Meta Heuristics, TSP Algorithms(B&B, Cutting Plain, Nearest Neighbour, Reversal Heuristic, Tabu, Simulated Annealing, Genetic), Deterministic & Dynamic Programming.

UNIT III

Markov Chains: Continuous Review Models, Single & Multi Period Models, Absolute & n-step Transition Probabilities, State in Markov Chain, First Passage Time, Analysis of Absorbing States.

Queuing Models: Elements of Queuing Model, Role of Exponential Distribution, Pure Birth & Death Model, Specialized Poisson Queues, P-K Formula, Queuing Decision Models.

UNIT IV

Simulation Modeling: Monte Carlo Simulation, Type of Simulations, Unconstrained Problems, Constrained Problems, Direct Search Method, Gradient Method, Separable, Quadratic, Chance-Constrained Linear Combinations & SUMT Programming Algorithms.

Text and Reference Books:

1. Operation Research By Taha – Pearson
2. Probability & Statistics with Reliability, Queuing & Computer Serine Application- Kishor S. Trivedi – Willey
3. Mathematical Modeling Principles & Applications:- CENGAGE Learning, Frank R. Giordano, William P. Fox.
4. Operation Research, K.Rajagopal – PHI
5. Operation Research Algorithms and Applications by Rathindra P.Sen, PHI

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-531-B DIGITAL VLSI DESIGN LAB

L	T	P	Credits
-	-	3	3

Class Work	:	20 Marks
Exams	:	30 Marks
Total	:	50 Marks

LIST OF EXPERIMENTS:

1. Design a CMOS inverter in schematic and simulate for Transient Characteristics.
2. Design a CMOS two input NAND gate, Two input NOR gate, Two input AND gate and Two input OR gate in schematic and simulate for Transient Characteristics.
3. Design the layout of a CMOS Inverter and simulate for DC (Transfer) and Transient characteristics.
4. Design the layout for two inputs NAND gate, two input OR gate, two input AND gate and two input NOR gate and simulate for DC (Transfer) and Transient characteristics.
5. Realized a two input EXOR gate in schematic, draw its layout and simulate for DC (Transfer) and Transient characteristics.
6. To realize a 1 bit full adder in CMOS schematic, design its layout using tool option and simulate for Transient Characteristics.
7. To realize a Boolean expression Y=Not ((A+B)(C+D)E) in schematic, draw its layout and simulate for Transient Characteristics..
8. To realize a 4 X 1 MUX using transmission gates in schematic and simulate for Transient Characteristics..
9. To Realize JK FLIPFLOP in CMOS schematic, design its layout and simulate for Transient Characteristics.
10. To Realize D FLIPFLOP and T FLIPFLOP in CMOS schematic, design its layout and simulate for Transient Characteristics.
11. To realize a four bit asynchronous counter using T flip-flop as a cell in schematic and simulate for Transient Characteristics.
12. To realize a four bit shift register using D flip-flop as a cell in schematic and simulate for Transient Characteristics.

NOTE:

7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTEC-505-B contents.

MTEC-537-B ADVANCED MICROPROCESSORS & APPLICATIONS LAB

L	T	P	Credits			
-	-	3	3	Class Work	:	20 Marks
				Exams	:	30 Marks
				Total	:	50 Marks

(A few experiments may be designed & included in this list depending upon the infrastructure available in the institute)

1. To study the architecture of Microprocessor 8086 Kit
2. Write an ALP to convert a hexadecimal No. to decimal No. in single step execution (DEBUG)
3. Write an ALP to enter a word from keyboard and to display
4. Write an ALP for addition of two one digit Numbers.
5. Write an ALP to display a string
6. Write an ALP reverse a string
7. Write an ALP to check whether the No. is Palindrome
8. To study the MIcrocontroller Kit
9. Write an ALP to generate 10 KHz frequency square wave
10. Write an ALP to generate 10 KHz & 100KHz frequency using interrupt
11. Write an ALP to interface intelligent LCD display
12. Write an ALP to interface intelligent LED display
13. Write an ALP to Switch ON alarm when Microcontroller receive interrupt
14. Write an ALP to interface one microcontroller with other using serial / parallel communication.

NOTE:

7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTEC-507-B contents.

MTEC-502-B ADVANCED ELECTRONICS INSTRUMENTATION

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Sensors for transducers: Potentiometers, Differential Transformers, Resistance Strain Gauges, Capacitance Sensors, Eddy current sensors, Piezoelectric, photoelectric, RTD, Thermocouple Sensors.

Digital instruments: A/D & D/A converters & their types, Data loggers, significance of 3 ½ & 4½ digit, automation in digital instruments, DMM, Digital frequency meter, universal counter & their applications.

Unit II

Oscilloscopes & Signal Analyzers: Digital Storage oscilloscope & its features like Roll, Refresh & sampling rate, Application of DSO in communication, Sampling Oscilloscope, current trends in oscilloscope technology, Wave Analyzer & its Applications, FET analyzers & network analyzers: their applications.

Current trends in Digital Instrumentation: Introduction to special function Add on cards, Computer Aided Software Engineering (CASE) Tool & its use in designing & development of Automated Measuring Systems, interfacing IEEE cards, Intelligent & Programmable Instruments using computers.

UNIT III

Introduction to SCADA & PLC: Data acquisition system, evaluation of SCADA, communication technologies, monitoring and supervisory functions, Block diagram of PLC, programming languages, Ladder diagram, Functional block diagram, Applications, Interfacing of PLC with SCADA.

SCADA system components & Architecture: Schemes, Remote Terminal Unit, Intelligent Electronic Devices, Communication Network, SCADA server. Various SCADA Architectures: advantages and disadvantages of each system.

UNIT IV

PLC Programming: Instructions, operational procedures, PLC Registers: Characteristics of Registers, module addressing, holding registers, input registers, output registers. PLC Functions: Timer functions and Industrial applications, counters, counter function & industrial applications, Arithmetic functions, Number comparison functions, number conversion functions.

Virtual Instrumentation: Advantages, Block diagram & architecture of Virtual Instruments, Data Flow Techniques, graphical programming in data flow, development of virtual instruments using GUI, Real Time Systems.

Text and Reference Books:

1. Digital instrumentation, By Bouwens,A.J., MGH
2. Measuring systems-Application & Design, By Doebelin, MGH
3. Electronic measurements & instrumentation, by B. M. Oliver & J. M. Cage. MGH
4. SCADA supervisory control and data acquisition, by Stuart A Boyer
5. Programmable Logic Controllers – Programming Method and Applications by JR. Hackworth and F.D Hackworth Jr. – Pearson, 2004.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-504-B ADVANCE OPTICAL COMMUNICATION

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Introduction to optical fiber: Introduction to ray theory, theory of optical wave propagation ,optical fiber attenuation ,optical fiber absorption ,scattering and band losses ,classification of optical fiber ,dispersion, dispersion shifted fiber ,dispersion modified fibers, dispersion compensated fibers, optical fiber non linear effects.

Optical amplifier: Types of optical amplifier, Raman optical amplifiers, semiconductor optical amplifier, Erbium doped fiber amplifier, application:155Mb/s sonnet/OC3-stm transducer amplifier.

UNIT II

Optical transmitter and receiver: Introduction to multiplexer,32:1 2.488Gb/s multiplexer with clock generator (VSC 8131) external modulated laser diode , the effect of noise and power supply noise rejection ,10Gb /s DWDM optical transmitter

Introduction , Data pattern ,photo detector diodes, classification of optical receiver, optical receiver performance characteristics,

Optical transreceivers: Introduction ,LED transreceivers, LASER diode Trans receiver, design guide lines for optical channel transreceivers , high speed optical channel transreceivers.

UNIT III

Optical modulation: Introduction, The mach zander interferometer ,The mech zander (LINBO3)Optical modulator The MZLIBNO, design process, modulator drivers ,DSB laser diode with PMFs for external modulator.

Multiplexing : Introduction ,WDM, future optical devices for DWDM schemes, DWDM multiplexing AWG multiplexer/demultiplexer for DWDM system add/drop multiplexer/demultiplexers,2.5 Gb/s 16:1 multiplexer.

UNIT IV

Optical system: Introduction ,optical power budget analysis ,10Mb/ soptical link designs for industrial applications, optical fiber link design, dispersion effect ,wave polarization effect in optical systems under sea optical system, soliton transmission.

Network: Introduction ,optical networks review of data communication links ,networks , network transport architecture ,LAN standards fiber channel asynchronous transfer mode , synchronous transfer mode.

Text Books:

1. Horal Kolimbris "fiber optical communication "Pearson

Reference Books:

1. John Gowar, "Optical Communication Systems", PHI
2. Gerd Keiser, "Optical Fiber Communication", TMH

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-506-B DIGITAL IMAGE PROCESSING

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Review of Digital Image Processing (DIP) Fundamentals and Filtering : Review of DIP basics and systems, sampling and Quantization, Representation of digital images, spatial and Gray-level resolution, Relationships between pixels: neighbours of pixel, Adjacency, connectivity, regions, and boundaries, distance measures, Image operations on a pixel basis.

Intensity Transformations and Spatial Filtering: Intensity Transformation Functions: Image negatives, log transformations, Power-Law (Gamma) transformations, piecewise –Linear Transformation functions; Histogram Processing: Histogram Equalization, Histogram Matching (Specifications), Local Histogram Processing, Using Histogram Statistics for Image Enhancement, spatial filtering: Spatial Correlation and Convolution, Vector Representation of Linear filtering, Generating Spatial Filter Masks, Smoothing Spatial Filters: Smoothing Linear Filters, Order Statistics (Nonlinear) Filters; Sharpening Spatial Filters: Using the second derivative for Image Sharpening-The Laplacian; Unsharp Masking and Highboost Filtering.

UNIT II

Image Filtering in Frequency Domain,Wavelets and MultiResolution Processing

Filtering in Frequency Domain: Relationship between the sampling and Frequency intervals, 2-D Impulse and shifting Properties, 2-D Sampling & 2-D Sampling Theorem, Aliasing in Images, 2-D Discrete-Fourier Transform and its Inverse, Properties of 2-D DFT, Additional Characteristics & Filtering Fundamentals in the frequency domain, correspondence between filtering in the spatial and frequency domains; Smoothing frequency domain filters: Ideal Lowpass Filters, Butterworth Lowpass Filters, Gaussian Lowpass Filters; sharpening frequency domain filters: Ideal Highpass Filters, Butterworth Highpass Filters, Gaussian Highpass Filters, Lapalacian in Frequency Domain; Unsharp Masking, Highboost Filtering, and High Frequency Emphasis Filtering, Homomorphic filtering, Implementation of DFT: computing 2-D DFT using 1-D DFT Algorithm, Computing IDFT using DFT Algorithm.

Wavelets and MultiResolution Processing: Introduction, Multiresolution Expansions, Wavelet Transforms in One Dimension: Wavelet Series Expansion, Discrete Wavelet Transform, Continuous wavelet transform, The Fast Wavelet Transform, Wavelet Transforms in two Dimensions, Wavelet Packets.

UNIT III

Image Restoration and Reconstruction

Restoration in presence of Noise only: A model of the image degradation/ restoration process, Noise models: Spatial and frequency properties of noise, some important noise probability density functions, Periodic Noise, Estimation of Noise Parameters; Restoration in the presence of noise only spatial filtering: Mean Filters, Order Statistic Filters, Adaptive Filters; Periodic noise reduction by frequency domain filtering: Bandreject Filters, Bandpass Filters, Notch Filters

Restoration in presence of Degradations: Linear, Position –Invariant Degradations, Estimating the Degradation Function: Estimation by Image Observation, Estimation by Experimentation, Estimation by Modeling; Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering

UNIT IV

Image Compression & Segmentation

Image Compression: Fundamentals: Coding Redundancy, Spatial and Temporal Redundancy, Irrelevant Information, measuring Image Information, Fidelity Criteria, Image Formats, Containers, and Compression Standards; Basic Compression Methods: Huffman Coding, Arithmatic Coding, LZW Coding, Run length Coding, Symbol Based Coding, Bit Plane Coding, Block Transform Coding, Predictive Coding, Wavelet Coding, Digital Image Watermarking.

Image Segmentation: Detection of Discontinuities: Point, Line, and Edge detection, Boundary detection, Thresholding: Role of Illumination, basic global thresholding, Optimum global thresholding using Otsu's method, Using Image Smoothing to improve global thresholding, Using Edges to improve global thresholding, Multiple thresholds, Variable Thresholding, Multivariable Thresholding, Regional –Based segmentation: Region growing, region splitting and merging, Segmentation Using Morphological Watersheds: Background, Dam Construction, Watershed Segmentation Algorithm, Use of Markers, use of motion in segmentation: Spatial Techniques, Frequency Domain Techniques.

Text and Reference Books:

1. Rafael C. Gonzalez and Richard E. Woods, "Digital Image Processing", Pearson
2. Anil K Jain, "Fundamentals of Digital Image Processing", PHI Edition 1997.
3. Keenneth R Castleman, " Digital Image Processing", Pearson
4. Chanda & Majumder, "Digital Image Processing & Analysis", PHI
5. M. K. Pakhira, "Digital Image Processing and Pattern Recognition", PHI.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-534-B ADVANCED OPTICAL COMMUNICATION LAB

L	T	P	Credits			
-	-	3	3	Class Work	:	20 Marks
				Exams	:	30 Marks
				Total	:	50 Marks

(A few experiments may be designed & included in this list depending upon the infrastructure available in the institute)

1. Study of optical devices.
2. Study of fiber optical detector.
3. Study of fiber optical transmitters
4. Determination of numerical aperture of optical fiber
5. Study of characteristics of LED.
6. Study of characteristics of LASER diode.
7. Setting a fiber optic analog link.
8. Setting a fiber optic digital link.
9. Study of modulation demodulation of light source by direct amplitude modulation techniques.
10. Forming a PC to PC communication link using optical fiber & RS 232.
11. Setting up a fiber optic voice link.
12. Study of modulation & Demodulation of light source by PPM technique.
13. Study of modulation & Demodulation of light source by PWM technique.
14. Study of Propagation loss & sending loss in optical fiber.

NOTE:
7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTEC-504-B contents.

MTEC-536-B ADVANCED IMAGE PROCESSING LAB

L	T	P	Credits
-	-	3	3

Class Work	:	20 Marks
Exams	:	30 Marks
Total	:	50 Marks

(A few experiments may be designed & included in this list depending upon the infrastructure available in the institute)

1. Take a hand written document, Perform pre-processing and try to segment into characters
2. Take an image, design fuzzy rules for content based image retrieval.
3. Take an image, design a neural network for content based image retrieval.
4. Write a program for image enhancement
5. Write a program for image compression
6. Write a program for color image processing
7. Write a program for image segmentation
8. Write a program for image morphology
9. Write a program for Image Restoration
10 Write a program for Edge detection
11. Write a program for Blurring 8 bit color versus monochrome

NOTE:
7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTEC-506-B contents.

MTEC-508-B ANALOG VLSI DESIGN

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

CMOS Models: Simple MOS large-signal model : Strong inversion, Weak inversion. Capacitance model, Small-signal MOS model, SPICE Level-3 model.

CMOS Sub circuits: MOS Switch, MOS Diode, MOS Active Resistors, CMOS Regulated Cascade current source, Cascade current sink .

UNIT II

Current Mirrors: **Passive and active current mirrors**, Simple current mirror, Cascode current Mirror, Widlar current mirror, Wilson Current Mirror

CMOS Amplifier: Single transistor Amplifiers stages: Common Drain, Common Gate & Common Source Amplifiers – resistive load, diode connected load, current source load, triode load, source degeneration, Simple Inverting Amplifier, Differential Amplifiers, Gilbert Cell, Cascade Amplifier, source follower, cascode amplifiers, Output Amplifiers

UNIT III

Operational Amplifier: Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, gain boosting, two stage MOS operational Amplifier with cascades, MOS Folded-cascade operational amplifiers, noise in op-amps, op-amp stability and frequency compensation.

Comparators: Comparators Models and Performance, Development of a CMOS Comparator, Design of a Two-Stage CMOS Comparator, Other Types of Comparators.

UNIT IV

Nonlinear Analog Circuits:

Voltage controlled oscillator, Comparators, Source Follower Phase Locked Techniques; Phase Locked Loops (PLL), Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters.

OTA & Switched Capacitor filters:

OTA Amplifiers, Sampling Switches, Switched Capacitor Circuits and Switched Capacitor Filters OTA

Text Books:

1. Paul B Gray and Robert G Meyer, "Analysis and Design of Analog Integrated Circuits".
2. Allen and Holberg – "*CMOS Analog Circuit Design"*

Reference Books

1. D. A. Johns and Martin, "Analog Integrated Circuit Design", John Wiley, 1997.
2. Gregorian and G C Temes, "Analog MOS Integrated Circuits for Signal Processing", John Wiley, 1986.
3. R L Geiger, P E Allen and N R Strader, VLSI Design Techniques for Analog & Digital Circuits, McGraw Hill, 1990.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-510-B MULTIMEDIA COMMUNICATION

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Multimedia & Information Representation

Multimedia Introduction: multimedia networks, Telephone networks, Data netwoks, Broadcast television networks, Integrated services digital networks, Broadband multiservice networks, types of Multimedia Applications: Movie on Demand, Near Movie on Demand, communication modes, multipoint conferencing, network QOS, Application QOS.

Multimedia Information Representation: Digitization principles, Encoder Design, Decoder Design, Unformatted Text, Formatted Text, Hypertext, Images: Graphics, Digitized documents, Digitized pictures; Audio: PCM speech, CD-qualty audio, Synthesized audio; Video: Broadcast television, Digital vedio, PC vedio, vedio content.

UNIT II

Text and Image Compression

Compression Principles & Text Compression: Compression Principles: Source encoders and Destination decoders, Lossless and lossy compression, Entropy encoding, Source encoding; Text Compression: Static Huffman coding, Dynamic Huffman Coding, Arithmatic Coding.

Image Compression: Graphics Interchange Format, Tagged image file format, digitized documents, digitized pictures.

UNIT III

Audio and Video compression: Audio Compression: Differential Pulse Code Modulation, Adaptive Differential PCM, Adaptive predictive coding, Linear Predictive coding, Code –excited LPC, Perceptual Coding, MPEG Audio coders, Dolby audio coders

Video compression: video compression principles, Motion Pictures Expert Group (MPEG), MPEG1, MPEG2.

UNIT IV

INTERNET AND DESIGNING FOR THE WORLD WIDE WEB

The internet and multimedia: The internet, Internetworking: Internet addresses, connections, The Bandwidth Bottleneck, Internet services, MIME-Types, The world wide web and HTML, Dynamic web pages and XML, multimedia on the web, Tools for the World Wide Web: web browsers, web servers, web page makers and site builders, plug-ins and delivery vehicles.

Designing For The World Wide Web: Developing for the web: HTML is a Markup Language, The Desktop Workspace, The Small Device Workspace, nibbling, Text for the web: making columns of text, flowing text around images; images for the web: GIF and PNG Images, JPEG Images, Using Photoshop, Backgrounds, clickable buttons, Client –side image maps, sound for the web, animation for the web.

Text Books:

1. Fred Halsall, "Multimedia Communications", Pearson
2. Tay Vaughan, "Multimedia, making it work" Eighth edition, Tata McGraw-Hill Edition
3.

Reference Books

1. Rao, Bojkovic & Milovanovic, "Multimedia Comm. System: Techniology , Std. & Network", PHI
2. John F. Koegel Bufod, "Multimedia Systems", Addison Wesley, Edition. 2000

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-512-B STATISTICAL SIGNAL PROCESSING

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Background: discrete-time signal processing, linear algebra, Mathematical preliminaries, Random variables & discrete-time random processes, Wiener filtering and MMSE estimates, Linear predication, Levinson-durbin algorithm and lattice, Classical detection and estimation theory, Statistical Models: Gaussian Distribution and relatives, Reproducing Distributions, Sample mean and variance, Fundamental of parametric and Linear Estimation,

UNIT II

Filters: Optimal Linear Filtering and Prediction, Overview of Spectral Estimation Methods. Adaptive Algorithms: 1)-LMS Algorithm, Convergence Analysis, Adaptive Noise Canceller, Lattice filters, Wiener filtering, Spectrum estimation, Adaptive filtering, Fundamentals of Detection, Detection Strategies for composite hypothesis,

UNIT III

Least Squares Algorithm: General Weighted Least Squares Methods, Recursive Least Squares Algorithm, Fast Least Squares Algorithm to AR modeling case

UNIT IV

Introduction to array processing, Composite Hypotheses in the Univariate Gaussian Model, Composite Hypotheses in the Multivariate Gaussian Model, Statistical Confidence Intervals,

Text and Reference Books:

1. Fundamentals of Statistical Signal Processing, Volume 1: Estimation Theory, Steven M.Kay
2. Discrete Random Signals and Statistical Signal Processing (Princeton Hall), Charles W.Therrien.
3. Statistical Signal Processing: Detection, Estimation and Time Series Analysis, Louis L.Scharf
4. An Introduction to Statistical Signal Processing, Robert M.Grey, Lee D.Davisson
5. Statistical Digital Signal Processing and Modeling, Monson H. Hayes, John Wiley, 1996

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-514-B DESIGN OF EMBEDDED SYSTEM

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Embedded Hardware And Software: Embedded system evolution trends, Terminology, Gates, Timing diagram, Memory, Microprocessor buses, Direct memory access, Interrupts, Built interrupts, Interrupts basis, Shared data problems, Interrupt latency, , Interrupt routines in an RTOS environment.

Embedded System Modelling With Hardware/Software Partitioning: Embedded systems, Hardware/Software Co-Design, Co-Design for System Specification and modelling- Single-processor Architectures & Multi-Processor Architectures, comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification, Hardware/Software Partitioning Problem, Hardware/Software Cost Estimation, Generation of Partitioning by Graphical modelling, Formulation of the HW/SW scheduling, Optimization.

UNIT II

Hardware/Software Co-Synthesis: The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

partitioning decision: Hardware / Software duality, coding Hardware, ASIC revolution, Managing the Risk, Co-verification, execution environment, memory organization, System start-up, Hardware manipulation, memory mapped access, speed and code density.

UNIT III

Concurrent Process Models And Hardware Software Co-Design: Modes of operation, Finite state machines, Models, HCFSL and state charts language, state machine models, Concurrent process model, Concurrent process, Communication among process, Synchronization among process, Implementation, Data Flow model, Design technology, Automation synthesis, Hardware software co-simulation, IP cores, Design Process Model.

Interrupt Service Routines: Watch-dog timers, Flash Memory basic toolset, Host based debugging, Remote debugging, ROM emulators, Logic analyser, Caches, Computer optimisation, Statistical profiling.

UNIT IV

Embedded Design Life Cycle: Product specification, Hardware/Software partitioning, Detailed hardware & software design, Integration, Product testing, Selection Processes, Microprocessor Vs Micro Controller, Performance tools, Bench marking, RTOS Micro Controller, RTOS availability, Tool chain availability, Other issues in selection processes.

In-Circuit Emulators & Testing: Buller proof run control, Real time trace, Hardware break points, Overlay memory, Timing constraints, Usage issues, Triggers, Bug tracking, reduction of risks & costs, Performance, Unit testing, Regression testing, Choosing test cases, Functional tests, Coverage tests, Testing embedded software, Performance testing, Maintenance.

Text and Reference Books:

1. David. E. Simon, "An Embedded Software Primer", Pearson Education, 2001.
2. T. Noergaard, "Embedded System Architecture, A comprehensive Guide for Engineers and Programmers", Elsevier.
3. Raj Kamal, "Embedded Systems- Architecture, Programming and Design", Tata McGraw Hill, 2006.
4. F. Vahid & T. Givargis "Embedded Systems Design: A Unified Hardware/Software Introduction", John & Wiley Pub.
5. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.
6. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub.
7. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice", Kluwer Academic Pub.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-516-B EMBEDDED NETWORKING

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Memory Interfacing: Memory: Memory write ability and storage performance, Memory types, composing memory, Advance RAM interfacing communication basic.

I/O INTERFACING: Microprocessor interfacing I/O addressing, Interrupts, Direct memory access, Arbitration multilevel bus architecture, Serial protocol, Parallel protocols, Wireless protocols, Digital camera example.

UNIT II

Embedded Communication Protocols: Serial/Parallel Communication, Serial communication protocols -RS232 standard, RS485, Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

USB AND CAN BUS: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets – Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT III

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT IV

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization – Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

Text and Reference Books:

1. Frank Vahid, Tony Givargis „Embedded Systems Design: A Unified Hardware/Software Introduction", John & Wiley Publications, 2002
2. Jan Axelson, "Parallel Port Complete: Programming, interfacing and using the PC's parallel printer port", Penram publications, 1996.
3. Dogan Ibrahim, "Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series", Elsevier 2008.
4. Jan Axelson „Embedded Ethernet and Internet Complete", Penram publications, 2003.
5. Bhaskar Krishnamachari, „Networking Wireless Sensors", Cambridge press 2005.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-518-B SEMICONDUCTOR DEVICE MODELLING

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Basic Semiconductor Physics: Energy Bands and Charge Carriers, Band Model, Bond Model, MOS Capacitor, Hall Effect. MOSFET and Compound Semiconductor FET, MOSFET capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF-modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling

UNIT II

Metal Semiconductor Junctions: Equilibrium in Electronic Systems, Ideal metal semiconductor junctions, Schottky Barriers, Mott barrier, tunnel contacts and ohmic Contacts.

BJT: Bipolar Junction Transistors, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors, Ebers-Moll Model, Hetero Junction Bipolar Transistor

UNIT III

Noise modeling: Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuits

Other MOSFET models : MOSFET Physical Effects , MOSFET High Field Effects, The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, noise model temperature effects, MOS model 9, MOSAI model

UNIT IV

Modeling of process variation and quality assurance: Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests.

Recent Developments in Microelectronic Devices.

Text and Reference Books:

1. S. M. Sze, *Modern Semiconductor Device Physics*, Wiley, 1998.
2. R. S. Muller and T. I. Kaminis, *Device Electronics for Integrated Circuits*, Second Edition, Wiley, 1986.
3. Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd.
4. Donald A. Neaman, " Semiconductor physicsand devices" Third Edition, McGraw–Hill Pvt Ltd,2007

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-520-B ADVANCE SATELLITE COMMUNICATION

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Introduction: Kepler's Laws of motion, Orbital aspects of Satellite Communications, Look Angle and Orbit determinations, Orbital effects in communication system Performance, Space craft subsystems, AOCS, TTC&M, Power system, Satellite transponder, spacecraft Antennas, Satellite Link Design-- System Noise temperature and G/T ratio - Design of downlink, Uplink - Design of satellite links for specified C/N, Implementation of error Detection on satellite links.

Multiple Access: FDMA, TDMA, CDMA, SSMA- comparison of multiple access techniques, Practical Demand Access systems, Multiple Access With on board processing.

UNIT II

Earth Station Technology: Earth Station Design, Design of Large Antennas, Tracking, Small earth station Antennas, Equipment for earth station; Satellite Packet Communications- Message transmission by FDMA: The M/G/1 Queue, Message transmission by TDMA - Pure ALOHA: Satellite packet switching - slotted ALOHA - Packet Reservation - Tree algorithm.

Overview of GPS: Basic concept, system architecture, space segment, user segment, GPS aided Geo-augmented navigation (GAGAN) architecture. GPS Signals: Signal structure, anti spoofing (AS), selective availability, Difference between GPS and GALILEO satellite construction.

UNIT III

GPS orbits and satellite position determination : GPS orbital parameters, description of receiver independent exchange format (RINEX) – Observation data and navigation message data parameters, GPS position determination.

GPS Errors : GPS error sources – clock error, ionospheric error, tropospheric error, multipath, ionospheric error estimation using dual frequency GPS receiver.

UNIT IV

Very small Aperture Terminal Networks: VSAT Technologies – Network Configurations - Multi access and Networking Network Error Control – Polling VSAT Networks; Mobile Satellite Networks--Operating Environment – MSAT Network concept - CDMA MSAT Network-Statistics of mobile propagation.

Phased Arrays in Radar and Communication Systems: System requirements for radar and communication antennas, Array characterization for radar and communication systems, Fundamental results from array theory, Array size determination.

Text Books:

1. T. Pratt and C.W., "Bostian Satellite Communications".
2. Tri T. Ha, "Digital Satellite Communication" (2 ed) 3 Robert J. Mailloux
3. B. Hoffman – Wellenhof, H. Liehtenegger and J. Collins, "GPS – Theory and Practice", Springer – Wien, New York (2001).

Reference Books:

1. James Ba – Yen Tsui, "Fundamentals of GPS receivers – A software approach", John Wiley & Sons (2001).
2. Phased Array Antenna Hand Book" , Artech House, Boston, London, 1994. 4.
3. Dr. D.C. Agarwal, "Satellite Communications" .

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-522-B MULTIRATE AND WAVELETS SIGNAL ANALYSIS

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

A Beginning with some practical situations, which call for multiresolution/ multiscale analysis - and how time-frequency analysis and wavelets arise from them. Examples: Image Compression, Wideband Correlation Processing, Magnetic Resonance Imaging, Digital Communication.

Piecewise constant approximation - the Haar wavelet, Building up the concept of dyadic Multiresolution Analysis (MRA). Relating dyadic MRA to filter banks, A review of discrete signal processing, Elements of multirate systems and two-band filter bank design for dyadic wavelets.

UNIT II

Families of wavelets: Orthogonal and biorthogonal wavelets, Daubechies' family of wavelets in detail, Vanishing moments and regularity, Conjugate Quadrature Filter Banks (CQF) and their design, Dyadic MRA more formally, Data compression - fingerprint compression standards, JPEG-2000 standards.

The Uncertainty Principle: and its implications: the fundamental issue in this subject - the problem and the challenge that Nature imposes, The importance of the Gaussian function: the Gabor Transform and its generalization; time, frequency and scale - their interplay, The Continuous Wavelet Transform (CWT), Condition of admissibility and its implications. Application of the CWT in wideband correlation processing.

UNIT III

Journey from the CWT to the DWT: Discretization in steps, Discretization of scale - generalized filter bank, Discretization of translation - generalized output sampling, Discretization of time/ space (independent variable) - sampled inputs.

Going from piecewise linear to piecewise polynomial, The class of spline wavelets - a case for infinite impulse response (IIR) filter banks.

UNIT IV

Variants of the wavelet transform and its implementational structures, The wavepacket transform, Computational efficiency in realizing filter banks - Polyphase components, The lattice structure, The lifting scheme.

An exploration of applications (this will be a joint effort between the instructor and the class).Examples: Transient analysis; singularity detection; Biomedical signal processing applications; Geophysical signal analysis applications; Efficient signal design and realization: wavelet based modulation and demodulation; Applications in mathematical approximation; Applications to the solution of some differential equations; Applications in computer graphics and computer vision; Relation to the ideas of fractals and fractal phenomena.

Text and Refrence Books:

1. L. Debnath.. Wavelet Transforms and Their Applications, Birkhauser Pub.
2. E. Mallat.. A Wavelet Tour of Signal Processing, Elsevier, Indian Ed.
3. Yves Meyer.. Wavelets and Operators, Cambridge Univ. Press.
4. G. Kaiser.. A Friendly guide to Wavelets, Birkhauser

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-524-B DSP PROCESSORS

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Introduction To Dsp Processors: Advantages of DSP, characteristics of DSP systems, classes of DSP applications, DSP processor embodiment and alternatives, Fixed Vs Floating point processors, fixed point and Floating point Data Paths.

DSP Architecture: An introduction to Harvard Architecture, Differentiation between Von-Neumann and Harvard Architecture, Quantization and finite word length effects, Bus Structure, Central Processing Unit, ALU, Accumulators, Barrel Shifters, MAC unit, compare, select, and store unit (CSSU), data addressing and program memory addressing

UNIT II

Memory Architecture: Memory structures, features for reducing memory access required, wait states, external memory interfaces, memory mapping, data memory, program memory and I/O memory, memory mapped registers.

Addressing & Instruction set: Various addressing modes - implied addressing, immediate data addressing, memory direct addressing, register direct and indirect addressing, and short addressing modes, Instruction types, various types registers, orthogonality, assembly language and application development.

UNIT III

Execution Control And Pipelining: Hardware looping, interrupts, stacks, pipelining and performance, pipelining depth, interlocking, branching effects, interrupt effects, instruction pipelining.

PERIPHERALS: Serial ports, timers, parallel ports, bit I/O port, host ports, communication ports, on-chip A/D and D/A converters, external interrupts, on chip debugging facilities, power consumption and management.

UNIT IV

Processors: Architecture and instruction set of TMS320C3X, TMS320C5X, TMS320C6X, ADSP 21XX DSP Chips, some example programs.

Recent Trends In Dsp System Design: FPGA-based DSP System Design, advanced development tools for FPGA, Development tools for Programmable DSPs, Code Composer Studio.

Text and Refrence Books:

1. Lapsley, P.Bier, J.Shoham, A. and Lee, E.A. DSP Processor Fundamentals: Architecture and Features, IEEE Press Series on Signal Processing, IEEE(2000)
2. Venkataramani, B. and Bhaskar, M., Digital Signal Processor: Architecture, Programming and Applications, TMH(2003)

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-526-B COMMUNICATION NETWORK

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Communication Networking Techniques: Communication Networks, Circuit Switching, Message Switching, Packet Switching, Local Networking Technology, The bus / tree topology, the ring topology, Medium Access control protocols (CSMA/CD, Token ring, FDDI, DQDB).

Propagation path-loss models: Mechanism, free space path loss, log-distance path loss models, Okumara model, Hata model, PCS model, Wideband PCS microcell model, indoor propagation models, Jake's channel model, Multi path characteristics of radio waves, signal fading, Time dispersion, Doppler spread, coherence time LCR, fading statistics, diversity techniques.

UNIT II

Wireless systems and standards: GSM standards, signaling and call control, mobility management, location tracing, wireless data networking, packet error modeling on fading channels, wireless data services, IS-95, GPRS.

Mobile Network Layer: Mobile IP (Goals, assumptions, entities and terminology, IP packet delivery, agent advertisement and discovery, registration, tunneling and encapsulation, optimizations), Dynamic Host Configuration Protocol (DHCP).

UNIT III

Data Dissemination: Communications asymmetry, classification of new data delivery mechanisms, pushbased mechanisms, pull-based mechanisms, hybrid mechanisms, selective tuning (indexing) techniques.

Network Operating Systems: Overview of network operating systems (Windows NT/Unix/Linux), Mobile IP33N Operating System.

UNIT IV

Mobile Ad hoc Networks (MANETs): Overview, Properties of a MANET, spectrum of MANET applications, routing and various routing algorithms, security in MANETs.

Vehicular Ad Hoc Networks (VANET): VANET architecture, Basic principles and applications of VANETs, Information dissemination in VANETs, brief introduction to vehicular mobility modeling for VANETs, challenges in VANETs, difference between VANETs and MANETs, overview of controller area network (CAN), DSRC (dedicated short range communications),Routing Protocols in Vehicular Ad Hoc Networks, optimization algorithm (PSO).

Text Books:

1. Computer Networking by Andrew Tanenbaum.
2. Mobile communications by Jochen H. Schiller, Wesley
3. VANET: Vehicular Applications and Inter-Networking Technologies by Hannes Hartenstein, Kenneth Laberteaux, john willey and sons
4. Advances in Vehicular Ad-Hoc Networks: Developments and Challenges by Mohamed Watfa, IGI Global

Reference Books:

1. Data And Computer Communication by William Stallings, Prentice Hall, 4th Ed.
2. Data communications and networking by Forouzan
3. Wireless Communications: Principles and practices by T. S. Rappaport, PHI 1996.
4. Principles and Applications of GSM - byV K Garg Prentice Hall
5. William C. Y. Lee, " Mobile Cellular Telecommunications, Analog and Digital Systems", 2nd ed, MGH-1995.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-601-B ADVANCED WIRELESS COMMUNICATION SYSTEM

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

An Introduction to Wireless Communication Systems : Introduction, Evolution of Mobile Radio Communication , Beginning of Radio, Wireless Mobile Communication, Applications of Wireless Communication , Disadvantages of Wireless Communication Systems , Examples of Wireless Communication Systems , Difference Between Fixed Telephone Network and Wireless Telephone Network , Development of Wireless Communication ,Fixed Network transmission Hierarchy , Comparison of Wireless Communication Systems.

Modern Wireless Communication Systems : Introduction, First Generation (1G), Second Generation (2G), Generation (2.5G) , Third Generation (3G), Evolution from 2G to 3G, Fourth Generation (4G), Digital Cellular System Parameter, Differences Between Analog Cellular and Digital Cellular Systems, Wireless Local Loop [WLL], Wireless Local Area Networks (WLANs) , PAN (Personal Area Network), Bluetooth.

UNIT II

Radio Wave Propagation: Introduction , Doppler Shift, Parameters of Multipath Channels, Fading, Diversity Techniques, Space Propagation Model, Phenomena of Propagation, Interleaving, Propagation Models; Outdoor Propagation Models: Longley-Rice model, Durkin's Model, Okumura Model, Hata Model, Walfisch and Bertoni Model, Indoor Propagation Models; Log-distance Path Loss Model; Ericsson Multiple Breakpoint Model

Cellular System Design Fundamentals: Introduction, Frequency Reuse, Cellular Capacity Increasing Parameters, Channel Assignment Strategies ,Hand-off Strategies, Hand-off Initiation, Type of Hand-off on the Basis of Decision-making Process,Channel Assignment Strategies for Hand-off, Interference , Tracking, Trunking, Grade of Service.

UNIT III

Cellular Mobile Systems: Introduction, Spectrum Allocation, ITU (International Telecommunication Union) , Wireless Communication System, Basic Components of Cellular Systems, Cellular System Architecture; CDMA, Physical and logical channels of IS -95 CDMA: Introduction, Physical Channels, Modulation, Bit Repetition, Block Interleaving, Channel coding Logical Channels, Paging Channels, access channels, Forward Traffic channels, Reverse Traffic Channels. GSM: Most Popular Cellular System, Type of Channels, Cell Concept in Wireless Communication, Shape Selection of the Cell.

CDMA as a protocol – Multiple Access Techniques: classification of multiple access protocols – contention less (scheduling) multiple access protocols – contention (random) multiple access protocols – Code division multiple access (CDMA) protocols - CDMA system concepts – spread spectrum multiple access – Code generation – DSCDMA with imperfect power control – Near – far effect – multi user interference in the reverse link and forward link.

UNIT IV

Wireless Networking : Introduction, Difference Between Fixed Telephone Network and Wireless Telephone Network, PAN (Personal Area Network), Technology Used, OSI Model, TCP/IP Model, Integrated Services Digital Network (ISDN), Traffic Routing in Wireless Networks, Routing Services, Types of Switching, Switching Techniques, X.25 Protocol, Data Services in Wireless Network, Network Architecture,

Advanced Intelligent Networks: Introduction, Advanced Intelligent Networks (AIN), Intelligent Networking (IN), SS7 Protocol (Signaling System # 7), Component Used in IN/AIN Architecture, Working of AIN , Difference Between IN and Succeeding AIN/IN, Intelligent Cell Concept, Zone Divided Power Delivery Intelligent Cells, Processing Gain Intelligent Cells, Applications of Intelligent Cell Concept, Advantages of Intelligent Cells Implementation

Text Books:

1. T.S. Rappaport, "Wireless Communication, Principles & Practice," Pearson Education.
2. Rajeshwar Dass, "Wireless Communication Systems," I.K International Pvt. Ltd
3. Mobile Communication: Jochen Schiller Pearson Education.

Reference Books

1. Kaveh Pahlavan & Allen H. Levesque, "Wireless Information Networks", Wiley series in Telecommunications and Signal processing
2. Kamilo Feher: Wireless Digital communications, Modulation and Spread S

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-603-B RELIABILITY ENGINEERING

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Introduction: Study of reliability and maintainability, concepts terms and definition, random events, bayes' formula, random variables, discrete distribution, binomial distribution, Poisson distribution, continuous distribution

Basic Reliability model: Reliability function, mean time to failure, hazards rate function, bath tab, conditional reliability, constant failure rate model, time dependent failure model.

UNIT II

Data collection and empirical method: Data collection, Empirical Method, Ungrouped complete data, grouped complete data, ungrouped censored data, group censored data, static life estimation

Reliability Testing: product testing, reliability life testing, test time calculation, length of test, burn in testing, acceptance testing, experimental design, reliability growth process, idealized growth curve, Duane Growth Model, AMSAA Model.

UNIT III

Failure and Repair Distribution: candidate distribution, probability plots and least square curve fitting, parameter estimation, confidence intervals, parameter estimation for covariance model.

Goodness to fit test: Chi Square Goodness Of fit test, Bast letts test for exponential distribution, Mann's Test for Weibull Distribution, Kolmogosov Smirnov test for normal, Log normal Distribution, Test for Power Law process model, On fitting distribution.

UNIT IV

Reliability Estimation and Applications: Redundancy, burn in testing, preventive main furnace analysis, Reliability Allocation, Reliability growth testing, Repairable system analysis, multiply censored data.

Implementation: Objectives function and processes the economics of reliability and maintain ability and system design organisational consideration, data source and data collection methods, product reliability, warranties & related matters, Software Reliability.

Text Books:

1. Reliability and Maintain Ability Engineering. Charles E. Ebeling TMH.

Reference Books

1. System Eng. And analysis, PHI Blanchard B. S & W. J.Fabrycky.
2. Engineering Reliability: New Techniques & applications. Dhillon B.S & C. Singh. John Wiley
3. Reliability centred maintenance, Mc Grow Hill New York by Smith, A. M.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-631-B ADVANCED WIRELESS COMMUNICATION SYSTEM LAB

L	T	P	Credits
-	-	3	3

Class Work	:	20 Marks
Exams	:	30 Marks
Total	:	50 Marks

LIST OF EXPERIMENTS:

1. Frequency Offset Estimation and Correction
2. Properties of Antennas: Polarization, Cross Polar Discrimination
3. Antenna Resonance and Gain Bandwidth measurement
4. Characterization of Fading Effects
5. Fading Counter-measures using Antenna diversity and Frequency diversity
6. Delay Spread Measurement
7. Handover Demonstration
8. Detailed receiver and transmitter parameters of a typical radio communication system – SINAD, fidelity, image rejection, modulation sensitivity, transmission bandwidth etc.
9. PC2PC communication – protocol standards, frame/ packet/ UDP structure etc
10. Multiple channel DSSS – spreading, dispreading, decoding etc.
11. Horn, micro strip antenna – radiation pattern, gain etc.
12. Microwave phase shifter – calibration.
13. Measurement of dielectric constants – solids & liquids.
14. OFDM Synchronization, Frequency Offset, and Channel Estimation.
15. OFDM Modulator and Demodulator

NOTE:
7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTEC-601-B contents.

MTEC-605-B CMOS MIXED SIGNAL CIRCUIT DESIGN

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

PLL: Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL,

Switched Capacitor Circuits: Switched Capacitor circuits - basic principles, some practical circuits such as switched capacitor integrator, biquad circuit, switched capacitor filter, switched capacitor amplifier, non-filtering applications of switched capacitor circuit such as programmable gate arrays, DAC and ADC, MOS comparators, modulators, rectifiers, detectors, oscillators.

UNIT II

Sampling Circuits: Sampling circuits: Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures: Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.

DAC: Input/output characteristics of an ideal D/A converter, performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, switching functions to generate an analog output corresponding to a digital input. D/A converter architectures: Resistor-Ladder architectures, current-steering architectures.

UNIT III

ADC: Input/output characteristics and quantization error of an A/D converter, performance metrics of A/D converter. A/D converter architectures: Flash architectures, two-step architectures, interpolate and folding architectures, pipelined architectures, Successive approximation architectures, interleaved architectures.

Filters: Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-C integrator, discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transfer function.

UNIT IV

Data Converter Snr: Quantization Noise, Signal to Noise Ratio, improving SNR by using Averaging and Feedback.

Mixed-Signal Layout Issues: Floor planning, Power Supply and Ground Issues, Fully Differential Design, Guard Rings, Shielding, Other Interconnect Considerations

Text and Reference Books:

1. Razavi, "Design of analog CMOS integrated circuits", McGraw Hill, 2001
2. Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000
3. Jacob Baker, "CMOS Mixed-Signal circuit design", IEEE Press, 2002
4. Gregorian, Temes, "Analog MOS Integrated Circuit for signal processing", John Wiley & Sons
5. Baker, Li, Boyce, "CMOS : Circuit Design, layout and Simulation", PHI, 2000

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-607-B MEMS AND IC INTEGRATION

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

MEMS and Microsystems: Overview of CMOS process in IC fabrication, MEMS system-level design methodology, Microfabrication Evolution, Microsystems miniaturization, Microsystem Applications in health care industry, aerospace industry, telecommunications.

Microsensors and Microactuation: Working principles of Microsystems, Microsensors – acoustic wave sensors, biomedical sensors, optical sensors, thermal sensors, Pressure sensors with embedded electronics(Analog/Mixed signal): Accelerometer with transducer, Gyroscope, RF MEMS, optical MEMS, Sensor noise calculation, Bolometer Design, Microactuation overview, Microactuation using thermal forces, electrostatic forces, shaped memory alloys, piezoelectric crystals, Microgrippers, Micromotors, Microvalves, Micropumps, Microaccelerometers, Microfluidics.

UNIT II

Microsystem Design- Mechanics Engineering: Equivalent Circuit representation of MEMS , signal conditioning circuits. Engineering Science and Engineering Mechanics for Microsystem Design

Microsystem Design- Thermofluid Engineering: Thermofluid engineering and microsystem design – fluid mechanics at macro and meso scale, fluid flow in nanoscale designs.

UNIT III

Scaling laws in Miniaturized Designs Scaling in electrostatic forces, electromagnetic forces, Scaling in electricity, fluid mechanics and heat transfer.

Microsystems fabrication processes Materials for MEMS and Microsystems, Photolithography, Ion Implantation, Diffusion, CVD, PVD, Epitaxy, Etching with reference to concers involved in microfabrication.

UNIT IV

Micromanufacturing Bulk Micromanufacturing, Surface Micromachining, LIGA Process

Micropackaging Microsystem Packaging, Interfaces in Microsystem Packaging, Packaging Technologies, Three dimensional packaging, Microsystems assembly, Selection of Packaging Materials

Text Books:

1. Gregory T.A. Kovacs, Micromachined Transducers Sourecbook, The McGraw-Hill, Inc. 1998
2. Stephen D. Senturia, Microsystem Design, Kluar Publishers, 2001
3. Nadim Maluf, An Introduction to Microelectromechanical Systems Engineering, Artech House, 2000.
4. M.H. Bao, Micro Mechanical Transducers, Volume 8, Handbook of Sensors and Actuators, Elsevier, 2000.
5. H. J. De Los Santos, Introduction to Microelectromechanical (MEM) Microwave Systems, Artech, 1999.

Reference Books:

1. Masood Tabib-Azar, Microactuators, Kluwer, 1998.
2. Ljubisa Ristic, Editor, Sensor Technology and Devices, Artech House, 1994
3. D. S. Ballantine, et. al., Acoustic Wave Sensors, Academic Press, 1997
4. James M.Gere and Stephen P. Timoshenko, Mechanics of Materials, 2nd Edition, Brooks/Cole Engineering Division, 1984

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-609-B ALGORITHM FOR VLSI DESIGN

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Logic synthesis & verification:
Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.
Partitioning: problem formulation, cost function and constraints, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

UNIT II

Floor planning & pin assignment: Floor planning model and cost function, Classification of Floor planning, constraint based floor planning, Integer Programming Based Floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.
Placement: problem formulation, cost function and constraints, simulation base placement algorithms, Partitioning Based Placement Algorithms, other placement algorithms,
.

UNIT III

Global Routing: Grid Routing and Global routing, Problem formulation, cost function and constraints, classification of global routing algorithms, routing regions, sequential global routing, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, Integer Programming Based Approach, Hierarchical Global Routing, Global Routing by Simulated Annealing
Detailed routing: problem formulation, cost function and constraints, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

UNIT IV

Over the cell routing & via minimization: Over-the-cell Routing: Cell Models, two layers over the cell routers, Three-Layer Over-the-cell Routing, constrained & unconstrained via minimization.
Compaction: problem formulation, Classification of Compaction Algorithms one-dimensional compaction, two dimension based compaction, hierarchical compaction

Text and Reference Books:

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.
2. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI
3. Design", KAP, 2002.
4. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition.
5. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

NOTE:
In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-611-B SOFTWARE FOR EMBEDDED SYSTEMS

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

EMBEDDED LINUX, WIN C.

UNIT II

TINY OS:

Review Of Operating Systems: Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes –Introduction to Distributed operating system – Distributed scheduling.

UNIT III

Overview Of RTOS 9: RTOS Task and Task state - Process Synchronisation- Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronisation problem – Deadlocks

Real Time Models And Languages: Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT IV

Real Time Kernel: Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

Rtos Application Domains: RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

Text and Reference Books:

1. Raj Kamal, "Embedded Systems- Architecture, Programming and Design" Tata McGraw Hill, 2006.
2. Herma K., "Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic, 1997.
3. Charles Crowley, "Operating Systems-A Design Oriented approach", McGraw Hill 1997.
4. C.M. Krishna, Kang, G.Shin, "Real Time Systems", McGraw Hill, 1997.
5. Raymond J.A.Bhur, Donald L.Bailey, "An Introduction to Real Time Systems", PHI 1999.
6. Mukesh Sighal and N. G. Shi "Advanced Concepts in Operating System", McGraw Hill 2000.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-613-B EMBEDDED APPLICATIONS BASED ON ADVANCED MICROCONTROLLERS

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

UNIT I

Introduction of Embedded Systems: Definition, ingredients of embedded system, requirements & challenges of embedded system design, different types of microcontrollers: Embedded microcontrollers, external memory microcontrollers etc., processor architectures: Harvard V/S Princeton, CISC V/S RISC, microcontrollers memory types, microcontrollers features: clocking, i/o pins, interrupts, timers, and peripherals.

Software For Embedded System Design: Development tools/ environments, Assembly language programming style, Interpreters, High level languages, Intel hex format object files, Debugging.

UNIT II

AVR Microcontroller: Introduction to AVR microcontroller, features of AVR family microcontrollers, different types of AVR microcontroller, architecture, memory access and instruction execution, pipelining, program memory considerations, addressing modes, CPU registers, Instruction set, and simple operations.

Features Of AVR Microcontroller: Timer: Control Word, mode of timers, simple programming, generation of square wave, Interrupts: Introduction, Control word Simple Programming, generation of waveforms using interrupt, serial interface using interrupt, Watch-dog timer, Power-down modes of AVR microcontroller, UART, SRAM.

UNIT III

ARM Architecture And Programming: Arcon RISC Machine, Architectural Inheritance, Core & Architectures, Registers, Pipeline, Interrupts, ARM organization, ARM processor family, Co-processors, Instruction set, Thumb instruction set, Instruction cycle timings.

ARM Programming: The ARM Programmer's model, ARM Development tools, ARM Assembly Language Programming and C-compiler programming.

UNIT IV

Arm Application Development: Introduction to DSP on ARM, FIR Filter, IIR Filter, Discrete fourier transform, Exception Handling, Interrupts, Interrupt handling schemes, Firmware and bootloader, Example: Standalone, Embedded Operating Systems, Fundamental Components.

Design with ARM Microcontrollers: Integrated development environment, Standard I/O Libraries, User Peripheral Devices, Application of ARM processor: Wireless Sensor Networks, Robotics.

Text and Reference Books:

1. Daniel Tabak, "Advanced Microprocessors", McGraw Hill. Inc., 1995.
2. Steave Furber, "ARM system - on - chip architecture", Addison Wesley, 2000.
3. John.B..Peatman, "Design with PIC Micro controller", Pearson Education, 1988.
4. Steve Furber, "ARM system on chip architecture", Addison Wesley, 2000.
5. Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield, "ARM System Developer's Guide Designing and Optimizing System Software", Elsevier 2007.
6. Trevor Martin, "The Insider's Guide To The Philips ARM7-Based Microcontrollers, An Engineer's Introduction To The LPC2100 Series" Hitex (UK) Ltd.,
7. Dananjay V. Gadre, Programming and Customizing the AVR microcontroller", McGraw Hill 2001
8. ARM Architecture Reference Manual 6. LPC213x User Manual

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions selection at least one question from each unit.

MTEC-633-B **SEMINAR**

L	T	P	Credits			
-	-	2	2			

Class Work	:	50 Marks
Exams	:	--
Total	:	50 Marks

The objectives of the course remain:

- To learn how to carry out literature search
- To learn the art of technical report writing
- To learn the art of verbal communication with the help of modern presentation techniques

A student will select a topic in emerging areas of Engineering & Technology and will carry out the task under the supervision of a teacher assigned by the department.

He/ She will give a seminar talk on the same before a committee constituted by the chairperson the department. The committee should comprise of 2 or 3 faculty members from different specializations. The teacher(s) associated in the committee will each be assigned 2 hours teaching load per week.

However, supervision of seminar topic will be in addition to the regular teaching load.

MTEC-637-B DISSERTATION (PHASE-I)

L	T	P	Credits
-	-	6	6

Class Work	:	100 Marks
Exams	:	--
Total	:	100 Marks

The primary objective of this course is to develop in student the capacity for analysis & judgment and the ability to carry out independent investigation in design /development through a dissertation work involving creativity, innovation and ingenuity. The work must start with comprehensive literature search and critical appreciation thereof so as to select research problem the student wishes to work on.

Each student will carry out independent dissertation under the supervision of some teacher(s) who will be called Supervisor(s). In no case more than two supervisors can be associated with one dissertation work.
The dissertation involving design/ fabrication/ testing/ computer simulation/ case studies etc. which commences in the III Semester will be completed in IV Semester. The evaluation of the dissertation phase –I besides approval of the dissertation topic of the students will be done by a committee constituted as under:

Chairperson of Department	: Chairperson
M Tech Coordinator/ Sr Faculty	: Member Secretary
Respective dissertation supervisor	: Member

The student will be required to submit two copies of his/her report to the department for record (one copy each for the department and participating teacher).

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MTEC-602-B DISSERTATION

L	T	P	Credits
-	-	20	20

Class Work	:	50 Marks
Exams	:	100 Marks
Total	:	150 Marks

The dissertation started in III Semester will be completed in IV Semester and will be evaluated in the following manner.

Internal Assessment

Internal Assessment (class work evaluation) will be effected as per ordinance through interim report, presentation and discussion thereon by the following committee of three persons:

Chairperson of Department	: Chairperson
M Tech Coordinator/ Sr Faculty	: Member Secretary
Respective dissertation supervisor	: Member

External Assessment

Final dissertation will be assessed by a panel of examiners consisting of the following:

Chairperson of Department	: Chairperson
Respective Supervisor(s)	: Member(s)
External expert	: To be appointed by the University

NOTE: The External Expert must be from the respective area of specialization. The chairperson & M Tech Coordinator with mutual consultation will divide the submitted dissertations into groups depending upon the area of specialization and will recommend the list of experts for each group separately to the V C for selecting the examiners with the note that an external expert should be assigned a maximum of FIVE dissertations for evaluation.

The student will be required to submit THREE copies of his/her report to the M Tech Coordinator for record and processing.